



Desert Microtechnology Associates, Inc.

Excellence in Semiconductor Development, Production & Technology

D17IP04 – 3rd Order Digital Filter

February 2017 Rev 0.0

Features

- 40 db attenuation
- Operates up to 2 MHz
- 256 clock latency
- Optimized to minimize power and area

Technology

- XH035 ISMOS

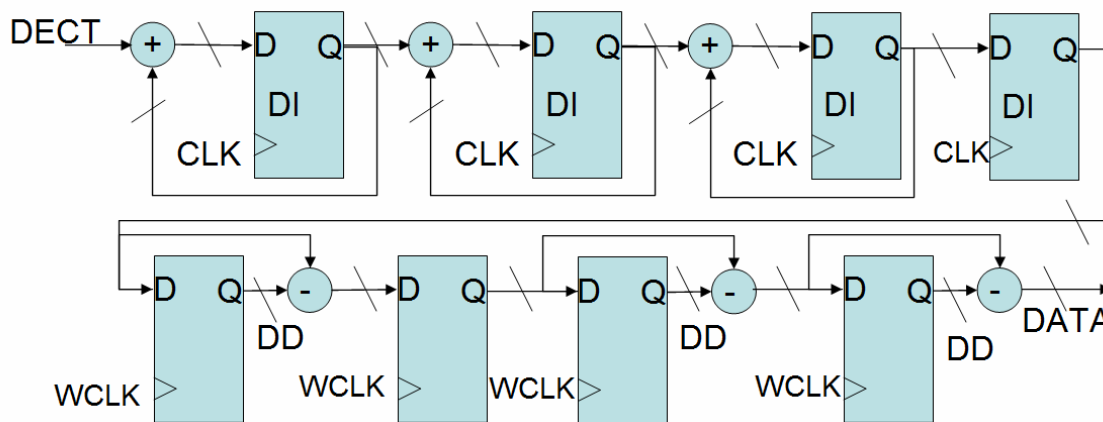
Applications

- 2nd order Delta-Sigma modulators
- Digital signal processing
- Incremental ADC

Deliverables

- Schematic
- Netlist, upon request
- GDSII

Functional Block Diagram



Description

The D17IP04 is a 3rd order cascade of integrators and comb, or differentiators, (CIC) digital filter. It converts a single channel digital bit stream into a 16 bit output word with a 256 clock latency. The design is optimized for area and power. It can operate down to 2V.



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Pin Description

| Name | Functional Description | Type | Default |
|-----------|---|--------|-------------|
| DECT | Digital bit stream input | Input | Active high |
| MDS | Input clock and data enable | Input | Active high |
| CLK | Bit rate clock, 2MHz or less | Input | Active high |
| WCLK | Work clock, should be CLK/64 and synchronized to CLK | Input | Active high |
| DFC[19:0] | Digital output word. For best performance, use DFC[17:2] for the final digital word | Output | Active high |
| VCC | Positive Supply Voltage | Supply | 3V |
| VSS | Negative Supply Voltage | Supply | 0V |