

0.18 µm Process Family:

> XS018



0.18 Micron Modular Image Sensor enabled CMOS Logic and Analog Technology

DESCRIPTION

XS018 is X-FAB's specialized process for fast image sensors. The optional available modules for 4 transistor cells, pinned photo diodes and the stitching capabilities make this technology ideal for large image sensor applications needing high frame rates as used for instance for medical and scientific X-ray cameras.

The 3.3V core module allows a low mask count

designs. The industrial standard single poly with up to six metal layers 0.18-micron drawn gate length N-well process can also be used for low power SOC application in the automotive, industrial and medical markets.

Comprehensive design rules, precise SPICE models, analog and digital libraries, IPs and development kits support the process for major EDA vendors.

KEY FEATURES OVERVIEW

- 0.18-micron single poly, up to six-metal N-well CMOS basic process
- Modular concept, 8" wafers
- 3.3V core module for low mask count
- Optional 1.8V module for high density logic (up to 125000 gates per mm²)
- 4T pixels with pinned photo diode for image sensors
- Planar passivation to support post processing of filter and micro lenses
- Isolation well for all 1.8V and 3.3V MOS devices
- High capacitive Metal-Insulator-Metal capacitors
- High capacitance Double MIM & Triple MIM Capacitors
- Thin top metal for image sensor applications
- I/O cell library with 2kV HBM ESD protection
- Typical and worst-case models - BSIM3v3.24 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterized & included in model
- Cadance, Mentor, Synopsys and Tanner PDK support
- Operating Conditions: Tj = -40°C ... +125°C

APPLICATIONS

- Large image sensors for X-Ray or industrial
- Mixed signal embedded systems/ systems on a chip (SOC) with image sensors
- Standard Logic/Controller circuits
- High Precision mixed signal circuits
- Low power mixed signal circuits

QUALITY ASSURANCE

X-FAB spends a lot of effort to improve the product quality and reliability and to provide comprehensive support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by

strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, ISO TS 16949 and other standards.

DELIVERABLES

- PCM tested wafers
- Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Service (MLM)
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development

DIGITAL LIBRARIES

- Foundry-specific optimized libraries
- Low power library for energy efficient and small size digital blocks
- Junction isolated library for low noise applications
- Liberty™ synthesis models
- IEEE 1364 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models

PRIMITIVE DEVICES

- NMOS/PMOS Transistors (1.8V & 3.3V)
- Isolated NMOS/PMOS Transistors (1.8V & 3.3V)
- Bipolar Transistors
- Poly Resistors, Diffusion Resistors, Metal Resistors
- MIM Capacitors
- High Capacitance MIM Capacitors
- Fringe Capacitors
- Junction Diodes

4T PIXEL

- Pinned photo diode
- Low Vt NMOS
- Buried channel NMOS

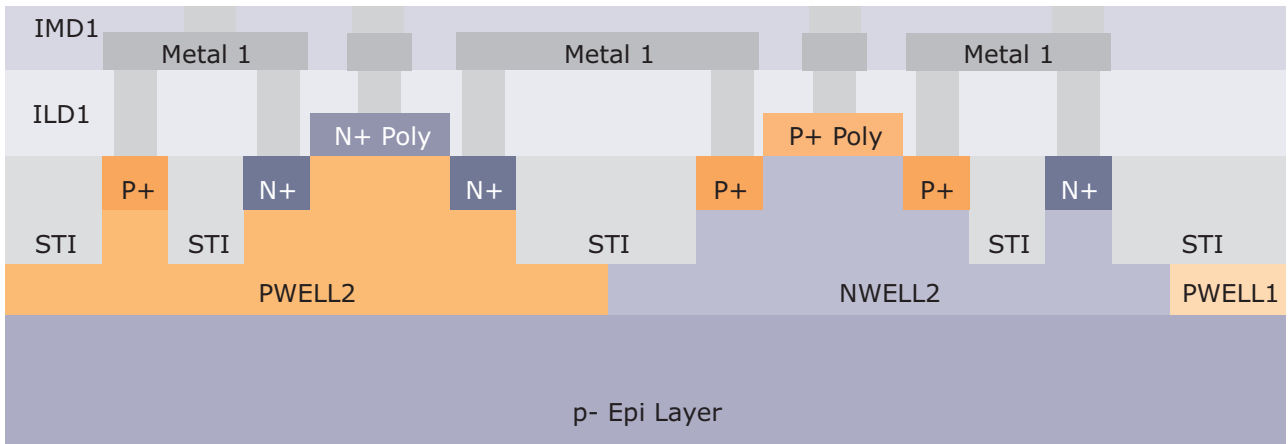
XS018 BASIC DESIGN RULES

Mask	width [μm]	Spacing [μm]
N-well	0.86	1.4
Active Area	0.22	0.28
Poly-silicon Gate	0.18	0.25
Poly-silicon Resistor	0.44	0.44
Contact	0.22	0.25
Metal 1	0.23	0.23
Via 1, 2, 3, 4	0.26	0.26
Metal 2, 3, 4, 5	0.28	0.28
Top Via	0.36	0.35
Top Metal	0.44	0.46

XS018 METAL OPTIONS

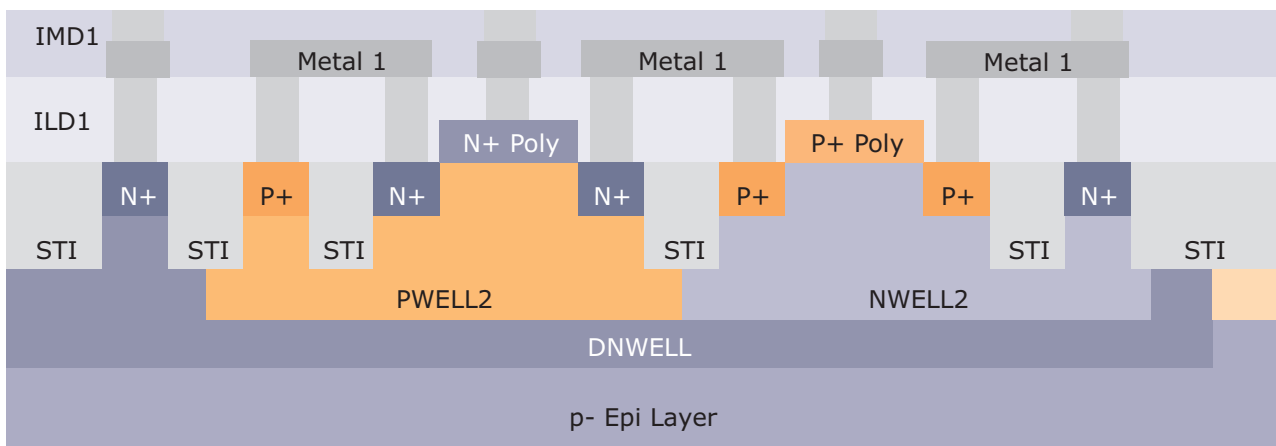
Number of Metals	Available Metal Layer Combinations	Module Names
2	MET1 - MET2	MOS3LP/MOS3ST+METTHIN
3	MET1 - MET2 - MET3	MOS3LP/MOS3ST+MET3+METTHIN
3	MET1 - MET2 - METTP	MOS3LP/MOS3ST+METMID
4	MET1 - MET2 - MET3 - MET4	MOS3LP/MOS3ST+MET3+MET4+METTHIN
4	MET1 - MET2 - MET3 - METTP	MOS3LP/MOS3ST+MET3+METMID
5	MET1 - MET2 - MET3 - MET4 - MET5	MOS3LP/MOS3ST+MET3+MET4+MET5+METTHIN
5	MET1 - MET2 - MET3 - MET4 - METTP	MOS3LP/MOS3ST+MET3+MET4+METMID
6	MET1 - MET2 - MET3 - MET4 - MET5 - METTP	MOS3LP/MOS3ST+MET3+MET4+MET5+METMID

XS018 DEVICES SCHEMATIC CROSS SECTION



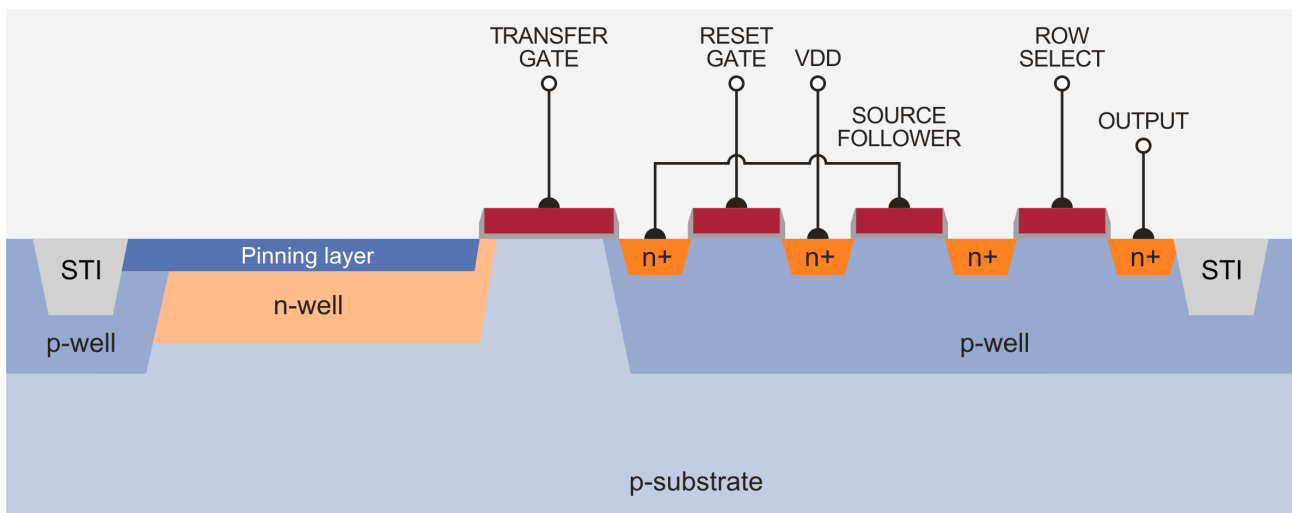
ne3
3.3V Low Power CMOS

pe3



ne3i
Isolated 3.3V Low Power CMOS

pe3i



4T Pixel

XS018 PROCESS FLOW

Core Module	Additional Modules	
Wafer Start		
Active area	Deep N WELL	ISOMOS
	Buried Channel	BCH
3.3V wells	1.8V wells	MOSLP/ MOSST
	3.3V wells	LVTN3B/C/D/E/F
Dual gate oxide	N-type transfer gate	4TPIX
	Poly silicon gate	
3.3V NMOS LDD	LDN WELL + buried pinning	PPDA/B/C/D
	1.8V NMOS LDD	MOSLP/ MOSST
	1.8V PMOS LDD	MOSLP/ MOSST
3.3V PMOS LDD		
Source/Drain implants	MRPOLY implant	MRPOLY
Salicidation		
Contact		
Metal 1		
Via 1		
Metal 2		
Single MIM capacitor		MIM23/ MIMH23
	Double MIM capacitor	DMIM/ DMIMH
Triple MIM capacitor		TMIM/ TMIMH
Via 2		MET3
Metal 3		
Single MIM capacitor		MIM34/ MIMH34
Double MIM capacitor		DMIM/ DMIMH
Triple MIM capacitor		TMIM/ TMIMH
Via 3		MET4
Metal 4		
Triple MIM capacitor		TMIM/ TMIMHM
Via 4		MET5
Metal 5		
MIM capacitor		MIM/ MIMH
Metthin		METTHIN
Top via		METMID
Top metal		
Planarized passivation		FLATPV
PAD		mask steps

XS018 CORE MODULE

Module Name	Descriptions	Masks No.
MOS3LP	Low Power 3.3V CMOS module	14
MOS3ST	Standard 3.3V CMOS module	14

XS018 ADDITIONAL MODULES

Module Name	Descriptions	Masks No.
MRPOLY	1k Ω /□ polysilicon resistor module	1
ISOMOS	Triple well isolated CMOS module	1
MOSLP	Low power 1.8V MOS module	5
MOSST	Standard 1.8V MOS module	3
LVTN3B	3.3V low threshold NMOS module	1
LVTN3C	3.3V low threshold NMOS module	1
LVTN3D	3.3V low threshold NMOS module	1
LVTN3E	3.3V low threshold NMOS module	1
LVTN3F	3.3V low threshold NMOS module	1
BCH	3.3V buried channel module	1
MIM	Single MIM capacitor module	1
MIM23	Single MIM capacitor module	1
MIM34	Single MIM capacitor module	1
DMIM	Double MIM capacitor module	1
TMIM	Triple MIM capacitor module	1
MIMH	Single high capacitance MIM capacitor module	1
MIMH23	Single high capacitance MIM capacitor module	1
MIMH34	Single high capacitance MIM capacitor module	1
DMIMH	Double high capacitance MIM capacitor module	1
TMIMH	Triple high capacitance MIM capacitor module	1
PPDA	Pinned-photo diode module	2
PPDB	Pinned-photo diode module	2
PPDC	Pinned-photo diode module	2
PPDD	Pinned-photo diode module	2
4TPIX	4T pixel module	0
METTHIN	Thin top metal module	0
MET3	3-metal module	2
MET4	4-metal module	2
MET5	5-metal module	2
METMID	Regular top metal module	2
FLATPV	Flat passivation	0
1DSTITCH	1D stitching	0
2DSTITCH	2D stitching	0

XS018 RESTRICTION FOR MODULE COMBINATIONS		
Module name	Use of the module also requires use of the following module(s)	Use of the module is not available with the use of the following module(s)
MOS3LP	METTHIN, METMID	MOS3ST
MOS3ST	METTHIN, METMID	MOS3LP
MOSLP		MOSST, MOS3ST
MOSST		MOSLP, MOS3LP
PPDA		PPDB, PPDC, PPDD
PPDB		PPDA, PPDC, PPDD
PPDC		PPDA, PPDB, PPDD
PPDD		PPDA, PPDB, PPDC
LVTN3B		LVTN3C, LVTN3D, LVTN3E, LVTN3F
LVTN3C		LVTN3B, LVTN3D, LVTN3E, LVTN3F
LVTN3D		LVTN3B, LVTN3C, LVTN3E, LVTN3F
LVTN3E		LVTN3B, LVTN3C, LVTN3D, LVTN3F
LVTN3F		LVTN3B, LVTN3C, LVTN3D, LVTN3E
4TPIX	PPDA, PPDB, PPDC, PPDD	
MIM	METMID	MIM23, MIM34, MIMH23, MIMH34, DMIM, TMIM, MIMH, DMIMH, TMIMH
MIM23	MET3	MIM34, MIMH23, MIMH34, MIM, DMIM, TMIM, MIMH, DMIMH, TMIMH
MIM34	MET4	MIM23, MIMH23, MIMH34, MIM, DMIM, TMIM, MIMH, DMIMH, TMIMH
DMIM	MET4, MET3+METMID	MIM23, MIM34, MIMH23, MIMH34, MIM, TMIM, MIMH, DMIMH, TMIMH
TMIM	MET5, MET4+METMID	MIM23, MIM34, MIMH23, MIMH34, MIM, DMIM, MIMH, DMIMH, TMIMH
MIMH	MET3, METMID	MIM23, MIM34, MIMH23, MIMH34, MIM, DMIM, TMIM, DMIMH, TMIMH
DMIMH	MET4, MET3+METMID	MIM23, MIM34, MIMH23, MIMH34, MIM, DMIM, TMIM, MIMH, TMIMH
TMIMH	MET5, MET4+METMID	MIM23, MIM34, MIMH23, MIMH34, MIM, DMIM, TMIM, MIMH, DMIMH
MET3	METTHIN, METMID	
MET4	MET3	
MET5	MET4	
METMID		METTHIN
1DSTITCH		2DSTITCH
2DSTITCH		1DSTITCH

Active Devices

XS018 MOS CORE TRANSISTORS

Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	IOFF [$\text{pA}/\mu\text{m}$]	BVDS [V]	Max. VDS [V]
1.8V native Vt NMOS	nn	MOS3ST MOS3LP	0.03	370			1.98
1.8V NMOS	ne	MOS3ST MOS3LP	0.45 0.47	600 475	< 50 < 3	> 3.6	1.98
1.8V PMOS	pe, pe_5*	MOS3ST MOS3LP	0.53 0.67	260 165	< 80 < 3	> 3.6	1.98
3.3V native Vt NMOS	nn3	MOS33ST MOS33LP	0.17	660			3.6
3.3V NMOS	ne3	MOS33ST MOS33LP	0.75 0.7	600 605	< 10 < 3	> 5	3.6
3.3V PMOS	pe3, pe3_5*	MOS33ST MOS33LP	0.66 0.64	310 300	< 10 < 3	> 5	3.6

* These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

XS018 ISOMOS TRANSISTORS

Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	IOFF [$\text{pA}/\mu\text{m}$]	BVDS [V]	max. VDS [V]
Iso. 1.8V NMOS	nei, nei_6*	MOS33ST+ISOMOS MOS33LP+ISOMOS	0.45 0.62	600 475	< 50 < 3	> 3.6	1.98
Iso. 1.8V PMOS	pei, pei_5*	MOS33ST+ISOMOS MOS33LP+ISOMOS	0.54 0.63	260 165	< 80 < 3	> 3.6	1.98
Iso. 3.3V NMOS	ne3i, ne3i_6*	MOS33ST+ISOMOS MOS33LP+ISOMOS	0.75 0.7	600 605	< 10 < 3	> 5	3.6
Iso. 3.3V PMOS	pe3i, pe3i_5*	MOS33ST+ISOMOS MOS33LP+ISOMOS	0.66 0.64	310 300	< 10 < 3	> 5	3.6

* These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

XS018 LOW VT TRANSISTORS

Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	IOFF [$\text{pA}/\mu\text{m}$]	BVDS [V]	max. VDS [V]	max. VGS [V]
3.3V buried ch NMOS	nb3	MOS33ST+BCH MOS33LP+BCH	0.09 0.1	805 800		> 5	3.6	3.6
Transfer gate	ne3tx	4TPIX	-	-	-	-	-	-
3.3V low Vt NMOS	nel3b*	MOS33ST+LVTB3B MOS33LP+LVTN3B	0.2 0.18	770 765	< 30	> 5	3.6	3.6
3.3V low Vt NMOS	nel3c*	MOS33ST+LVTN3C MOS33LP+LVTN3C	0.26	745 730	< 30	> 5	3.6	3.6
3.3V low Vt NMOS	nel3d*	MOS33ST+LVTN3D MOS33LP+LVTN3D	0.32 0.33	710 700	< 30	> 5	3.6	3.6
3.3V low Vt NMOS	nel3e*	MOS33ST+LVTN3E MOS33LP+LVTN3E	0.39 0.41	680 670	< 30	> 5	3.6	3.6
3.3V low Vt NMOS	nel3f*	MOS33ST+LVTN3F MOS33LP+LVTN3F	0.44 0.49	655 640	< 30	> 5	3.6	3.6

* Empty Netlist content was implemented into the PDK. Only use this device for LVS verification, do not use it for simulations.

Active Devices (Continued)

XS018 BIPOLAR TRANSISTORS							
Device	Name	Available	BETA	VA [V]	VBE [mV]	max. VCE [V]	VEB [V]
1.8V vPNP	qpva	MOSLP	2.8	100	710	1.98	1.98
	qpvb		2.9		669		
	qpvc		2.8		636		
1.8V vPNP	qpva	MOSST	2.5	100	710	1.98	1.98
	qpvb		2.6		669		
	qpvc		2.5		636		
3.3V vPNP	qpva3	MOS3LP	2.6	100	710	3.6	3.6
	qpvb3		2.5		669		
	qpvc3		2.7		635		
3.3V vPNP	qpva3	MOS3ST	2.75	100	710	3.6	3.6
	qpvb3		2.8		668		
	qpvc3		2.8		635		

Passive Devices

XS018 POLY RESISTORS					
Device	Name	Available with module	RS [Ω/\square]	Temp. Coeff. [$10^{-3}/K$]	Max VTB [V]
N+ Poly	rnp1, rnp1_3*	MOS3ST, MOS3LP	330	-1.38	3.6
P+ Poly	rpp1, rpp1_3*	MOS3ST, MOS3LP	290	-0.11	3.6
Lightly dope P+ Poly1	rpp1s, rpp1s_3*	MOS3ST, MOS3LP	6.3	2.92	3.6
Lightly dope P+ Poly1	rpp1k, rpp1k_3*	MRPOLY	1000	-0.9	3.6

* These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency. Parameters of these devices are identical to the corresponding basic device.

XS018 DIFFUSION RESISTORS						
Device	Name	Available with module	RS [Ω/\square]	Thickness/junc. depth [μm]	Temp. Coeff. [$10^{-3}/K$]	Max VTB [V]
1.8V N+ diffusion	rdn	MOSST, MOSLP	65		1.42	1.98
1.8V P+ diffusion	rdp	MOSST, MOSLP	135		1.23	1.98
1.8V N-well	rnw	MOSST, MOSLP	940	1.5	2.9	3.6
3.3V N+ diffusion	rdn3	MOS3ST, MOS3LP	62	0.2	1.42	3.6
3.3V P+ diffusion	rdp3	MOS3ST, MOS3LP	130	0.2	1.23	3.6
3.3V N-well	rnw3	MOS3ST, MOS3LP	940	1.5	2.9	3.6
1.8V LV NMOS SCR	rnw_scr *	MOSST, MOSLP	-	-	-	-
3.3V LV NMOS SCR	rnw3_scr *	MOS3ST, MOS3LP	-	-	-	-

* These devices are only allowed to be used for ESD protection. Please refer to ESDdocumentation on XTIC

Passive Devices (Continued)

XS018 METAL RESISTORS							
Device	Name	Available with module	RS [Ω / \square]	Thickness/junc. depth [μm]	Max J/W [$\text{mA}/\mu\text{m}$]	Temp. Coeff. [$10^{-3}/\text{K}$]	Max VTB [V]
Metal 1	rm1	MOS3ST, MOS3LP	0.095	0.555	1	3.2	3.6
Metal 2	rm2	MOS3ST, MOS3LP	0.085	0.555	1	3.2	3.6
Metal 3	rm3	MET3	0.085	0.555	1	3.2	3.6
Metal 4	rm4	MET4	0.085	0.555	1	3.2	3.6
Metal 5	rm5	MET5	0.085	0.555	1	3.2	3.6
Top Metal	rmtpt	METMID	0.043	0.975	1.6	3.2	3.6

XS018 MIM CAPACITORS							
Device	Name	Available with module	Area Cap [$\text{fF}/\mu\text{m}^2$]	V Coeff. [1/V]	BV [V]	max. VTB [V]	
Single MIM, M2/M3	cmm3	MIM23+MET3	1	15	> 20	3.6	
Single MIM, M3/M4	cmm4	MIM34+MET4	1	15	> 20	3.6	
Single MIM, M2/MTP Single MIM, M3/MTP Single MIM, M4/MTP Single MIM, M5/MTP	cmm3t cmm4t cmm5t cmm6t	METMID+MIM MET3+METMID+MIM MET4+METMID+MIM MET5+METMID+MIM	1	15	> 20	3.6	
Double MIM, M2/M3/MTP Double MIM, M2/M3/M4	cdmm4t cdmm4	MET3+METMID+DMIM MET4+DMIM	2	3	> 20	3.6	
Triple MIM, M2/M3/M4/MTP Triple MIM, M2/M3/M4/M5	ctmm5t ctmm5	MET4+ METMID+ TMIM MET5+TMIM	3	15	> 20	3.6	
High cap. MIM, M2/M3	cmmh3	MIMH23+MET3	2.2	-120	> 10	3.6	
High cap. MIM, M3/M4	cmmh4	MIMH34+MET4	2.2	-120	> 10	3.6	
High cap. MIM, M2/MTP High cap. MIM, M3/MTP High cap. MIM, M4/MTP High cap. MIM, M5/MTP	cmmh3t cmmh4t cmmh5t cmmh6t	METMID+MIMH MET3+METMID+MIMH MET4+METMID+MIMH MET5+METMID+MIMH	2.2	-120	> 10	3.6	
High cap. DMIM, M2/M3/MTP High cap. DMIM, M2/M3/M4	cdmmh4t cdmmh4	MET3+METMID+DMIMH MET4+DMIMH	4.4	-20	> 10	3.6	
High cap. TMIM M2/M3/M4/MTP High cap. TMIM M2/M3/M4/M5	ctmmh5t ctmmh5	MET4+METMID+TMIMH MET5+TMIMH	6.6	-120	> 10	3.6	

XS018 FRINGE CAPACITORS					
Device	Name	Available with module	Cell Cap [fF]	BV [V]	Max. VTB [V]
3.3V M1/M2/M3 fringe	csf3a	MET3	21.7	> 70	5.5
3.3V M1/M2/M3/M4 fringe	csf4a	MET4	29.9	> 70	5.5
3.3V M1/M2/M3/M4/M5 fringe	csf5a	MET5	38	> 70	5.5
3.3V M1/M2/M3/MTP fringe	csft4a	MET3+METMID	26.1	> 70	5.5
3.3V M1/M2/M3/M4/MTP fringe	csft5a	MET4+METMID	34.3	> 70	5.5
3.3V M1/M2/M3/M4/M5/MTP fringe	csft6a	MET5+METMID	42.4	> 70	5.5

Passive Devices (Continued)

XS018 JUNCTION DIODES						
Device	Name	Available with module	Area Cap [fF/ μm^2]	BV [V]	Leakage Current [fA/ μm^2]	Max VCC [V]
1.8V N+ diff. /PW1	dn	MOSLP, MOSST	1.12	> 6	5.0×10^{-4}	1.98
1.8V P+ diff. /NW1	dp	MOSLP, MOSST	0.98	> 6	5.0×10^{-4}	1.98
1.8V NW1 /Psub	dnw	MOSLP, MOSST	0.12	> 9	1.0×10^{-3}	3.6
3.3V N+ diff. /PW2	dn3	MOS3LP, MOS3ST	0.87	> 6	7.0×10^{-4}	3.6
3.3V P+ diff. /NW2	dp3	MOS3LP, MOS3ST	1	> 6	7.0×10^{-4}	3.6
3.3V NW2 /Psub	dnw3	MOS3LP, MOS3ST	0.12	> 9	1.0×10^{-3}	3.6
DNW /Psub	ddnw	ISOMOS	0.38	> 9	7.0×10^{-5}	3.6
1.8V PW1/DNW	dpw	ISOMOS + (MOSLP, MOSST)	0.7	> 9	5.0×10^{-4}	3.6
3.3V PW2/DNW	dpw3	ISOMOS	0.7	> 9	5.0×10^{-4}	3.6

XS018 PINNED PHOTO DIODES				
Device	Name	Available with module	Pinning Voltage [V]	Max Vcc [V]
Pinned photo diode (V _{pin} 0.75V)	dppda	PPDA	0.72	3.6
Pinned photo diode (V _{pin} 1.00V)	dppdb	PPDB	0.85	3.6
Pinned photo diode (V _{pin} 1.25V)	dppdc	PPDC	1.05	3.6
Pinned photo diode (V _{pin} 1.5V)	dppdd	PPDD	1.25	3.6

STANDARD CELL LIBRARIES

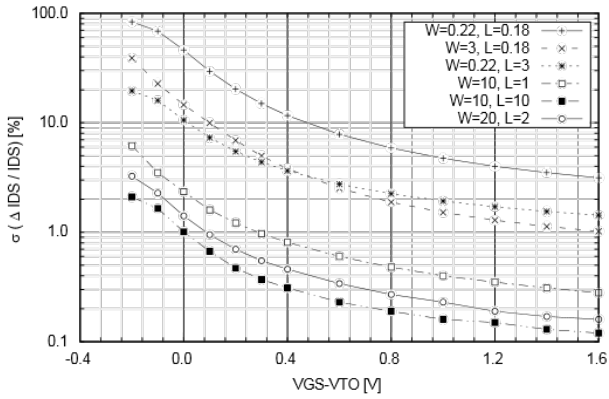
XS018 STD CELLS LIB			
Device	Library feature	Voltage range	Application benefits
D_CELLS	Standard, low power	1.2V/1.8V	High speed, low power cells available, P&R compatible with D_CELLS_LL
D_CELLS_LL	Low leakage, low power	1.2V/1.8V	Low leakage, low power cells available, P&R compatible with D_CELLS

I/O CELL LIBRARIES

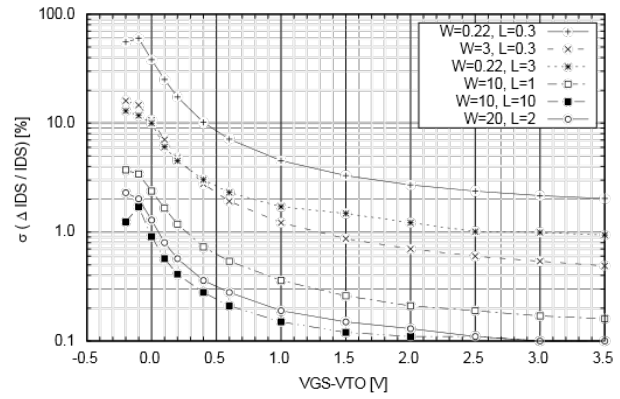
XS018 I/O LIBRARY					
Device	Library Feature	V _{CORE} *	V _{IO} *	ESD Level	Application benefits
IO_CELLS_FC1V8	Standard, V _{CORE} =V _{IO} single supply voltage	1.8V (1.2V)	1.8V (1.2V)	2kV HBM	Core limited
IO_CELLS_C1V8	Standard, V _{CORE} =V _{IO} single supply voltage	1.8V (1.2V)	1.8V (1.2V)	4kV HBM	Pad limited
IO_CELLS_FC1V8	Standard, V _{CORE} ≤V _{IO} multi supply voltage	1.8V	3.3V	2kV HBM	Core limited

* Please refer to the library databook for details about available PVT ranges

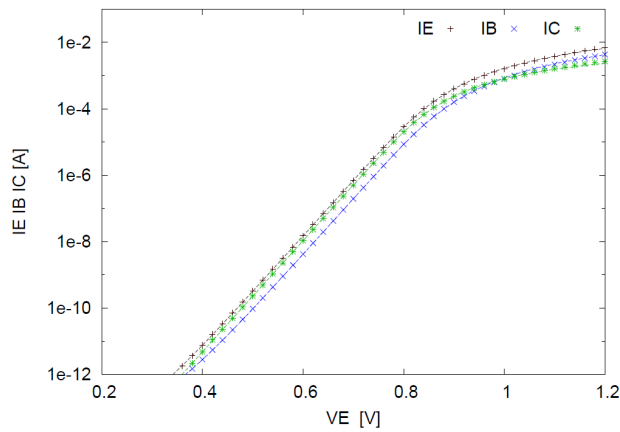
EXAMPLES FOR MEASURED AND MODELED PARAMETER CHARACTERISTICS



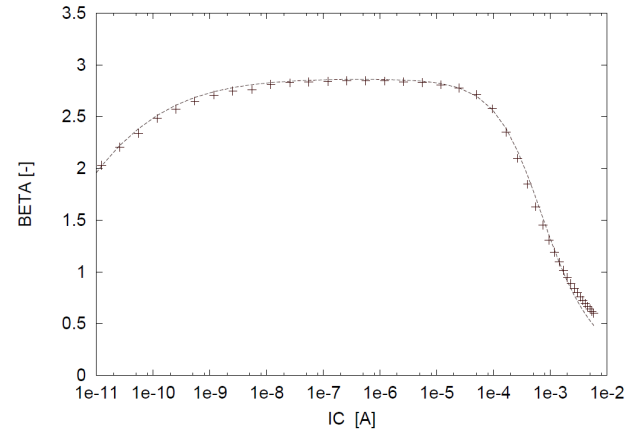
Device ne (MOSLP): drain current matching vs. VGS-VTO, (typical values, drawn W and L)



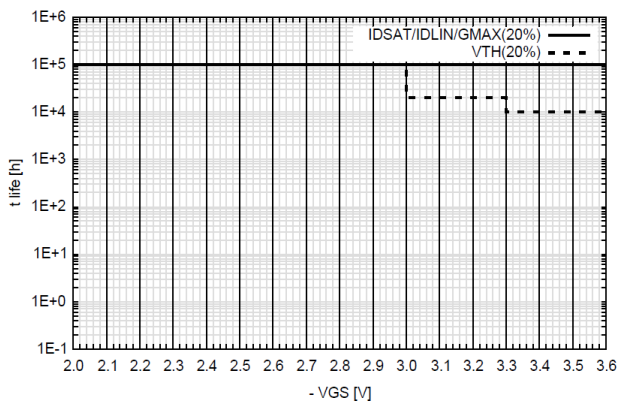
Device pe3 (MOS3ST): drain current matching vs. VGS-VTO, (typical values, drawn W and L)



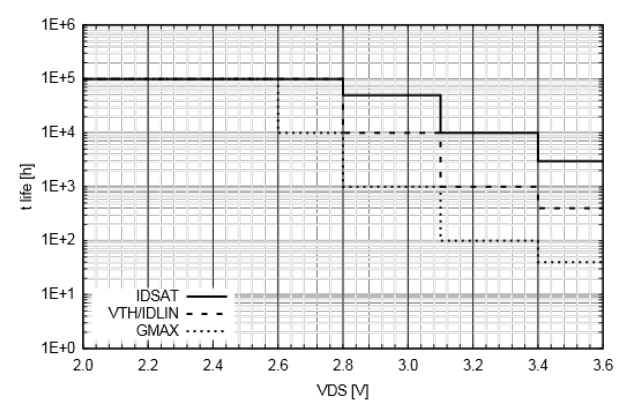
Gummel plot of 3.3V vertical PNP transistor qpva for a typical wafer, VC = VB = 0V, VE = 0 ... 1.2V, symbols = measured values, solid line = modelled



DC characteristic of 3.3V vertical PNP transistor qpvb3 for a typical wafer, VC = VB = 0V, VE = 0 ... 1.2V, symbols = measured values, solid line = modelled

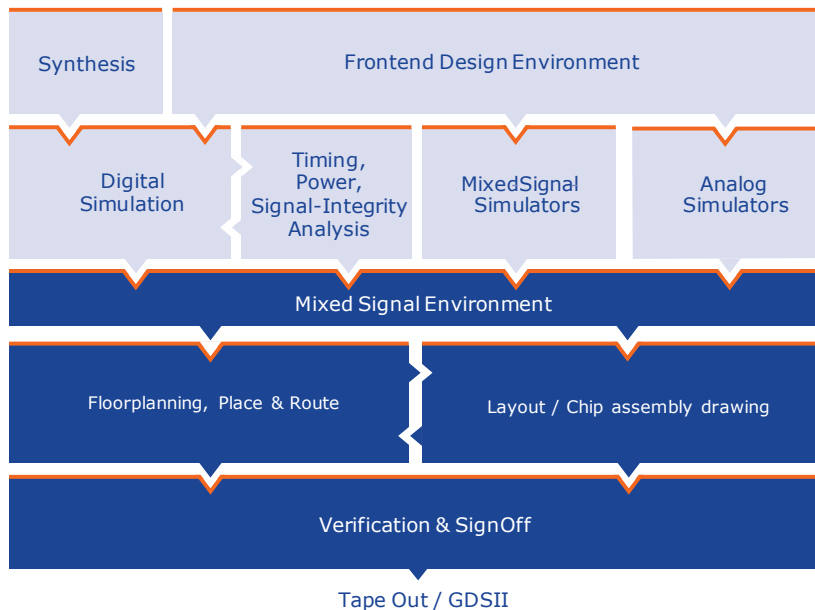


HCI DC lifetime plot for device pe3 (MOS3LP) for a typical wafer.



HCI DC lifetime plot for device nel3f for a typical wafer.

XS018 SUPPORTED EDA TOOLS



Note: Diagram shows overview of reference flow at X-FAB. Detailed information of supported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center X-TIC.

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which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well. The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

CONTACT

Marketing & Sales Headquarters
 X-FAB Semiconductor Foundries AG
 Haarbergstr. 67, 99097 Erfurt, Germany
 Tel.: 49-361-427 6160
 Fax: 49-361-427 6161
 Email: info@xfab.com
 Web: http://www.xfab.com

Technology & Design Support
 hotline@xfab.com
 Silicon Foundry Services
 sifo@xfab.com

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