

0.35 μm Process Family:

> XH035



0.35 Micron Modular Analog Mixed Signal Technology with RF capability and HV Extensions

DESCRIPTION

The XH035 series is X-FAB's 0.35-micron Modular RF capable Mixed Signal Technology. Main target applications are standard cell, semi-custom and full custom designs for Industrial, Automotive and Telecommunication products. Based on a single poly, triple metal 0.35-micron drawn gate length process for digital applications, process modules are available such as embedded Non-Volatile Memory, high voltage options, as well as standard or thick fourth layer metal, double-poly and MIM capacitor and high resistance polysilicon. Bipolar as well as MOS Transistors are available. Worldclass low noise

p-mos and n-mos transistors make this technology a first choice for application needing very low noise and high signal-to-noise ratios. A suite of RF active and passive components are also available. All main modules are comparable in Design Rules and Transistor Performance with other state of the art 0.35 μm CMOS Processes. Comprehensive design rules, precise SPICE models, analog and digital libraries, IP's and development kits support the process on platforms supplied by the major EDA tool vendors.

KEY FEATURES OVERVIEW

- 0.35-micron single poly, triple metal CMOS basic process with modular concept
- 3.3V Core, 5V tolerant I/O
- 5V dual gate or 5V only module
- Low threshold voltage option
- Low leakage process option
- Four layer metal options for high density circuits
- Thick top metal for inductors and Smart Power applications
- Benchmark setting Low noise p-mos and n-mos transistors
- Compact high-voltage devices with operating voltages of 45V (55V), 70V (75V) and 90V (100V)
- Core module EEPROM, programmable polyfuse
- High value poly resistor
- MIM, double MIM and stacked MIM & PIP capacitors with high capacitance area
- HV sandwich capacitors with extended operating voltage
- Special opto-modules to increase optical sensitivity and reduce dark current
- Integrated MEMS Pressure Sensors module.
- Polyimide module for stress relief & passivation protection
- High density up to 28000 gates per mm^2
- I/O cell library with 4kV HBM ESD protection levels
- Typical ad worst-case models - BSIM3v3.24 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterized & included in model
- Cadence, Mentor, Synopsys and Tanner PDK support
- Operating Conditions: $T_j = -40^\circ\text{C} \dots +125^\circ\text{C}$

APPLICATIONS

- Mixed-signal embedded systems / systems-on-chip (SOC)
- Low power mixed-signal circuits
- High Precision mixed-signal circuits
- RF applications
- Communications, consumer, automotive and industrial markets
- Low noise amplifiers for sensor interface circuits

QUALITY ASSURANCE

X-FAB spends a lot of effort to improve the product quality and reliability and to provide comprehensive support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by

strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, ISO TS 16949 and other standards.

DELIVERABLES

- PCM tested wafers
- Optional engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional design services: feasibility studies, Place & Route, synthesis, custom block development

DIGITAL LIBRARIES

- Foundry-specific optimized libraries
- Standard core library for high speed digital blocks
- IEEE 1364 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models
- Synthesis libraries
- Macrofunction and IPs on request
- RAM, DPRAM, ROM

ANALOG LIBRARIES

- Operational amplifiers
- Comparators
- Bandgaps
- Bias cells
- DAC/ADC
- RC oscillators
- Power-On-Reset
- HV cells
- RF building blocks

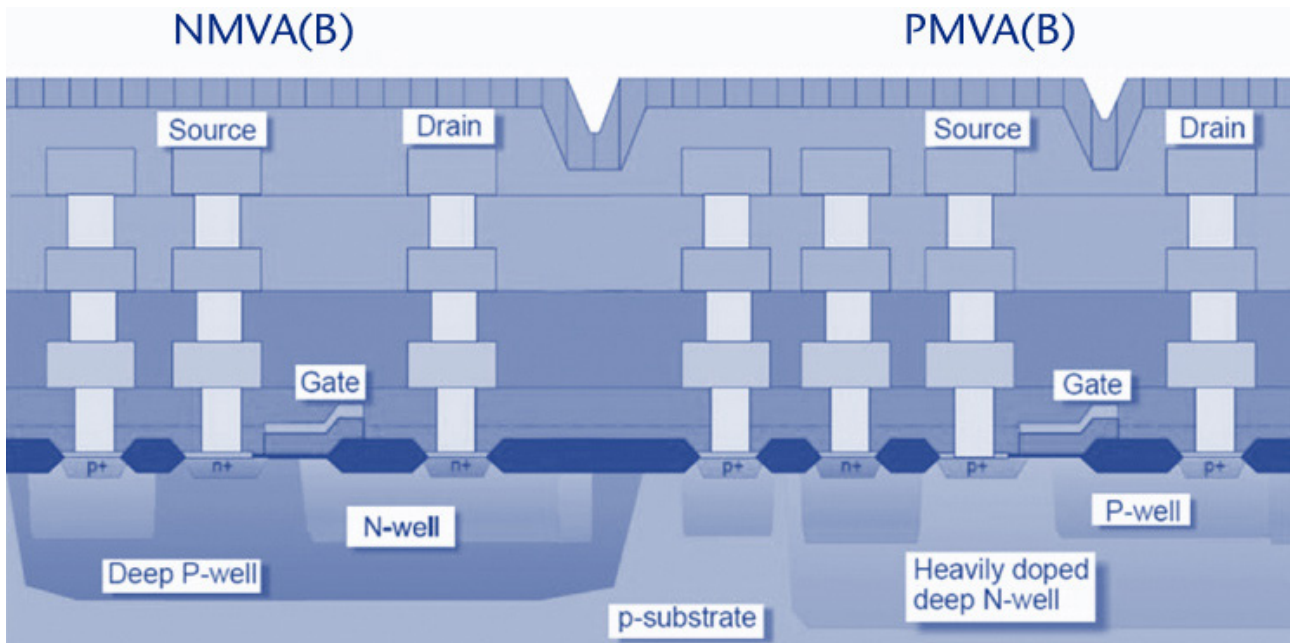
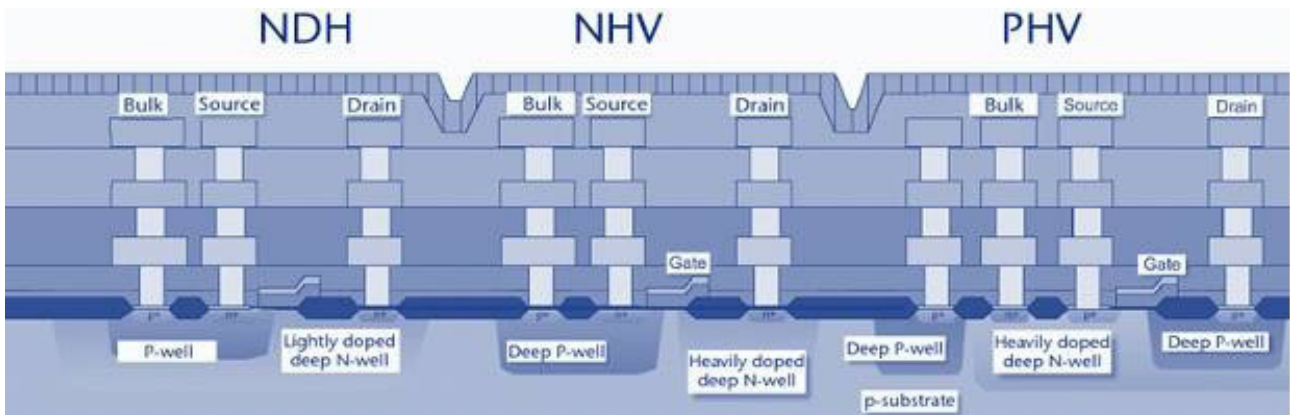
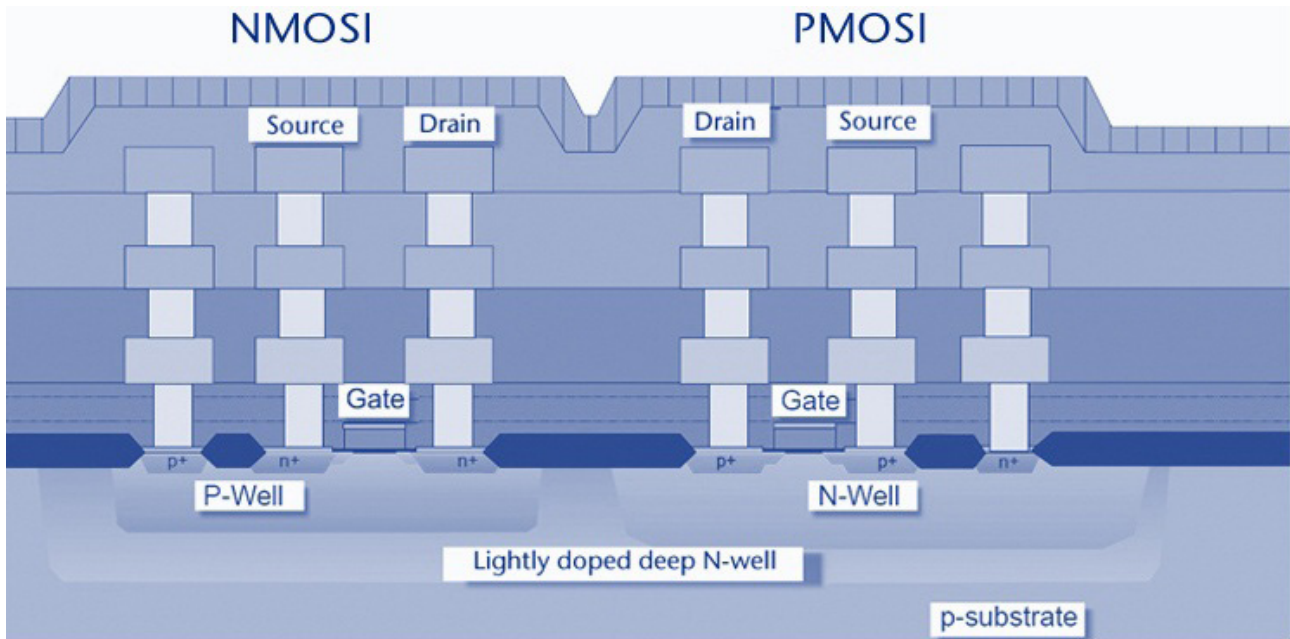
PRIMITIVE DEVICES

- NMOS/PMOS transistors
- Bipolar transistors
- Low noise NMOS
- Diodes
- Capacitors
- Resistors
- Inductors
- Varactors

XH035 BASIC DESIGN RULES

Mask	width [µm]	Spacing [µm]
N-well	1.6	1.0
Active Area	0.5	0.6
Poly-silicon Gate/Resistor	0.35	0.45
Contact	0.4	0.4
Metal 1, Via 1, 2, 3	0.5	0.45
Metal 2, 3	0.6	0.5 (0.6 if Top Layer Metal)
Metal 4	0.6	0.6
Thick Metal	3.0	2.5

XH035 DEVICES SCHEMATIC CROSS SECTION



XH035 PROCESS FLOW

MOS/MOSLT/MOSLL/MOS5 Basic/Common	MOS Additional	MOSLT/MOSLL Additional	MOS5 Additional
Zero Layer			DW Implant NHVEMID
	DW Implant		DW Implant HVMOS(MID/THK)
	DW Implant		NHVE(MID/THK)
		DW Implant	ISOMOS/PHOTODIO
	HDW Implant		THKOX
		DS Implant	THKOX/ISOMOS/PHOTODIO
	HV DW Implant		PHVE(MID/THK)/HVMOS(MID/THK)
Active Area		BN Implant	BURDIF
N-well			
N-Field			
	VP Implant		THKOX
		ESD PW Implant	NHVEMID/THK
	ESD PW Implant		NHVE(MID/THK)
	WN Implant		NMVMOS
	WP Implant		PMVMOS
	ND Implant		DEPL
	Dual Gate Oxide		MOS5A/THKOX/NHVE(MID/THK)/HVMOS(MID/THK)
		Thick Gate Oxide	THKOX
	High Res. Poly		HRPOLY
		Low Res. Poly	LRPOLY
Poly 1			
	5V N- Implant		MOS5A
N- Implant			not available with MOS5
5V N- Implant			MOS5 only
P- Implant			
		Poly 2	CAPPOLY
N+ Implant			
P+ Implant			
Silicide Block		Very High Resistance Poly	XRPOLY
Contact			
		DMIM Capacitor	DMIM
Metal 1			
Via 1			
		MIM Capacitor	MIM
Metal 2			
Via 2			not available with METAL2
		DMIM Capacitor	DMIM
Metal 3			not available with METAL2
		Via 3	
		Metal 4	METAL4/THKMET
	Optical Window		OPTO/OPTO_RED/OPTO_IR
Passivation		Flat Passivation	FLATPV
	Polyimide Deposition		PIMIDE
Back side grinding		Backside Etching (MEMS post processing)	IRPSENS

mask steps

XH035 PROCESS MODULES		
Module Name	Descriptions	Masks No.
MOS	Core MOS module	14
MOSLT	Low threshold MOS module	14
MOSLL	Low leakage MOS module	14
MOSS	Mid Gate oxide MOS module	13
CAPPOLY	Polysilicon 2 module	1
HRPOLY	High resistance polysilicon 1 module	1
XRPOLY	Very high resistance polysilicon 1 module	1
ISOMOS	Isolated MOS module	2
BURDIF	Buried N module	1
MOSSA	Mid Gate oxide module	3
THKOX	Thick Gate oxide module	3
DEPL	Depletion NMOS module	1
HVMOSMID	Mid gate oxide module (HV)	3 (2, if MOSS selected)
HVMOSTHK	Thick gate oxide module (HV)	3
NHVEMID	Mid gate oxide module (HV)	3 (2, if MOSS selected)
NHVETHK	Thick gate oxide module (HV)	3
NMVMOS	Medium voltage NMOS module	1
PMVMOS	Medium voltage PMOS module	1
PHVEMID	Mid gate oxide module (HV)	1
PHVETHK	Thick gate oxide module (HV)	1
PMVMOS	Medium voltage PMOS module	1
LNMOS	Low noise module	0
LRPOLY	Low resistance polysilicon	1
MIM	MIM capacitor module	1
DMIM	Double MIM capacitor module	1
METAL2	Top metal 2 module	-2
METAL4	Top metal 4 module	2
THKMET	Thick metal 4 module	2
THKMET3	Thick metal 3 module	0
OPTO	Optical window module	1
OPTO_RED	Optical window module optimized for red light	1
OPTO_IR	Optical window module optimized for infrared light	1
PIXEL	Pixel module	0
FLATPV	Flat passivation Module	0
PIMIDE	Polyimide module	1
IRPSENS	Integrated relative pressure sensor module	1
EEPROM	EEPROM module	0
TEEPROM	Tiny EEPROM module	0
CEEPROM	Core EEPROM module	0
OTP	OTP module	0

XH035 ADDITIONAL MASK COUNT FOR MODULE COMBINATION

Module Name	When combines with modules	Combined additional mask count
THKOX	ISOMOS	4
HVMOSMID	MOSS5A	5
HVMOSTHK	THKOX	5
NHVE MID	MOSS5A/ HVMOSMID	5
PHVE MID	HVMOSMID	2
NHVETHK	THKOX	4
NHVETHK	HVMOSTHK	5
PHVETHK	HVMOSTHK	2

XH035 RESTRICTION FOR MODULE COMBINATIONS 1

Module	MOS Required	MOS Not Allowed	MOSLL, MOSLT Required	MOSLL, MOSLT Not Allowed	MOSS Required	MOSS Not Allowed
MOSS5A		THKOX, HVMOSTHK, NHVETHK	NA*	NA*	NA*	NA*
THKOX		MOSS5A, HVMOSMID, NHVE MID	LRPOLY		NA*	NA*
NMVMOS	THKOX		THKOX		NA*	NA*
PMVMOS	THKOX		THKOX		NA*	NA*
HVMOSMID	ISOMOS	THKOX, HVMOSTHK, NHVETHK, PIXEL	NA*	NA*	ISOMOS	PIXEL
HVMOSTHK	ISOMOS	MOSS5A, HVMOSMID, NHVE MID, PIXEL	NA*	NA*	NA*	NA*
NHVE MID	ISOMOS	THKOX, HVMOSTHK, NHVETHK, PIXEL	NA*	NA*	ISOMOS	PIXEL
PHVE MID	NHVE MID		NA*	NA*	NHVE MID	
PHVETHK	NHVETHK		NA*	NA*	NA*	NA*
NHVETHK	ISOMOS	MOSS5A, HVMOSMID, NHVE MID, PIXEL	NA*	NA*	NA*	NA*
DEPL	THKOX		THKOX		NA*	NA*
BURDIF			LRPOLY			
CAPPOLY		PIXEL	LRPOLY			PIXEL
LRPOLY	NA*	NA*			NA*	NA*
HRPOLY			NA*	NA*		
XRPOLY	HRPOLY	OPTO, OPTO_IR, OPTO_RED, PIXEL		OPTO, OPTO_IR, OPTO_RED, PIXEL	HRPOLY	PIXEL
EEPROM	THKOX, NMV-MOS, PMVMOS, BURDIF	METAL2, THKMET3, PIXEL, FLATPV	THKOX, NMV-MOS, PMVMOS, BURDIF		NA*	NA*
TEEPROM	THKOX, BURDIF	METAL2, THKMET3, PIXEL, FLATPV	THKOX, BURDIF		NA*	NA*
CEEPROM		FLATPV, PIXEL			NA*	NA*
OTP	METAL4, HRPOLY	PIMIDE				

* NA = Not allowed with selected module

XH035 RESTRICTION FOR MODULE COMBINATIONS 2

Module name	Use of the module also requires use of the following module(s)	Use of the module is not available with the use of the following module(s)
MOS		MOSS, MOSLT, MOSLL
MOSS		MOS, MOSLT, MOSLL
MOSLT		MOS, MOSS, MOSLL
MOSLL		MOS, MOSS, MOSLT
MIM		DMIM, METAL2
DMIM	METAL4, THKMET	MIM, METAL2, THKMET3
METAL2		MIM, DMIM, METAL4, THKMET, THKMET3, EEPROM*, TEEPROM*, OPTO, OPTO_RED, OPTO_IR
METAL4		THKMET, THKMET3, METAL2
THKMET		METAL4, METAL2, THKMET3, OPTO, OPTO_RED, OPTO_IR, PIXEL, FLATPV
THKMET3		EEPROM*, TEEPROM*, METAL2, METAL4, THKMET, DMIM, OPTO, OPTO_RED, OPTO_IR, PIXEL, FLATPV
OPTO		MOSS, XRPOLY, METAL2, THKMET3, THKMET, PIMIDE, OPTO_RED, OPTO_IR, PIXEL, FLATPV
OPTO_RED		MOSS, XRPOLY, METAL2, THKMET, THKMET3, OPTO, OPTO_IR, PIMIDE, PIXEL, FLATPV
OPTO_IR	ISOMOS, THKOX	MOSS, XRPOLY, METAL2, THKMET3, THKMET, OPTO, OPTO_IR, PIMIDE, PIXEL, FLATPV
PIXEL		MOSLT, MOSLL, HVMOSMID, HVMOSTHK, NHVEMID, NHVETHK, DEPL, CAPPOLY, XRPOLY, EEPROM, TEEPROM, CEEPROM, THKMET3, THKMET, OPTO, OPTO_RED, OPTO_IR, PIMIDE, IRPSENS
FLATPV		MOSLT, MOSLL, EEPROM, TEEPROM, CEEPROM, THKMET3, THKMET, OPTO, OPTO_RED, OPTO_IR, PIMIDE, IRPSENS
PIMIDE		OPTO, OPTO_RED, OPTO_IR, PIXEL, FLATPV, OPT
IRPSENS		FLATPV, PIXEL

* The EEPROM and TEEPROM modules are not allowed with METAL2 or THKMET3 because EEPROM & TEEPROM blocks require the three metal layers METAL1, METAL2 and METAL3, but CEEPROM can be used with METAL2 or THKMET3.

XH035 METAL OPTIONS

Number of Metals	Available Metal Layer Combinations	Module Names
2	MET1 - MET2	(MOS/MOSS/MOSLL/MOSLT)+METAL2
3	MET1 - MET2 - MET3	(MOS/MOSS/MOSLL/MOSLT)
3	MET1 - MET2 - METL	(MOS/MOSS/MOSLL/MOSLT)+THKMET3
4	MET1 - MET2 - MET3 - MET4	(MOS/MOSS/MOSLL/MOSLT)+METAL4
4	MET1 - MET2 - MET3 - METL	(MOS/MOSS/MOSLL/MOSLT)+THKMET

Active Devices

XH035 MOS CORE TRANSISTORS							
Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	BVDS [V]	Max. VDS [V]	Max. VGS [V]
3.3V NMOS	nmos	MOS	0.60	500	> 5.5	3.6	3.6
		MOSLT	0.55	485			
		MOSLL	0.67	430			
3.3V PMOS	pmos	MOS	0.74	250	> 5.5	3.6	3.6
		MOSLT	0.50	240			
		MOSLL	0.73	175			
5V NMOS (mid oxide)	nmos5	MOS5, MOSSA	0.95	450	> 7	5.5	5.5
5V PMOS (mid oxide)	pmos5	MOS5, MOSSA	0.94	205	> 7	5.5	5.5
5V NMOS (thick oxide)	nmv	(MOS, MOSLT, MOSLL) +THKOX	1.15	150	> 8	5.5	5.5
5V PMOS (thick ox.)	pmv	MOS +THKOX (MOSLL, MOSLT) +THKOX	0.95	76 80	> 8	5.5	5.5
5V Native NMOS (thick ox.)	nnmv	THKOX	0.04	220	> 8	5.5	5.5
5V PMOS (thick ox., HV)	pmvic	NHVETHK	1.62	57	> 8	5.5	5.5

XH035 LOW NOISE TRANSISTORS						
Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	BVDS [V]	Max. VDS [V]
3.3V low noise NMOS	nmos_ln	MOS+LN MOS	0.66	280	> 5.5	3.6
3.3V isolated low noise NMOS	nmosi_ln, nmosi_ln_6, nmosi_ln_h_6	MOS+ISOMOS +LN MOS	0.64	285	> 5.5	3.6

XH035 RF TRANSISTORS						
Device	Name	Available with module	ft [GHz]	fmax [GHz]	Max. VDS [V]	Max. VGS [V]
3.3V NMOS for RF	nmosrf	MOS, MOSLL, MOSLT	25	40	3.6	3.6
			25	37		
3.3V PMOS for RF	pmosrf	MOS, MOSLT, MOSLL	15	24	3.6	3.6
			11	21		
Isolated 3.3V NMOS for RF	nmosirf, nmosirf_6, nmosirf_h_6	(MOS, MOSLL)+ISOMOS, MOSLT+ISOMOS	25	40	3.6	3.6
			25	37		
Isolated 3.3V PMOS for RF	pmosirf	MOS+ISOMOS, (MOSLT, MOSLL) +ISOMOS	15	24	3.6	3.6
			11	21		
5V NMOS thick oxide for RF	nmvrf	THKOX	7	24	5.5	5.5
5V PMOS thick oxide for RF	pmvrf	THKOX	4	15	5.5	5.5

Active Devices (Continued)

XH035 ISOMOS TRANSISTORS							
Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	BVDS [V]	max. VDS [V]	max. VGS [V]
Isolated 3.3V NMOS	nmosi, nmosi_6, nmosi_h_6	MOS +ISOMOS	0.59	500	> 5	3.6	3.6
		MOSLT +ISOMOS	0.50	500			
		MOSLL +ISOMOS	0.66	445			
Isolated 3.3V PMOS	pmosi	MOS +ISOMOS	0.78	240	> 5	3.6	3.6
		MOSLT +ISOMOS	0.51	245			
		MOSLL +ISOMOS	0.75	170			
Isolated 3.3V NMOS for HV isolation	nmosia, nmosia_6	MOS +(HVMOSMID, HV-MOSTHK)	0.58	500	> 5	3.6	3.6
Isolated 3.3V PMOS for HV isolation	pmosia	MOS +(HVMOSMID, HV-MOSTHK)	0.83	220	> 5	3.6	3.6
Isolated 3.3V PMOS for HV isolation	pmosib	MOS +ISOMOS	0.78	240	> 5	3.6	3.6
Isolated 3.3V NMOS for HV isolation	nmosic, nmosic_6	MOS +(NHVEMID, NHVETHK)	0.54	540	> 5	3.6	3.6
Isolated 3.3V PMOS for HV isolation	pmosic	MOS +(NHVEMID, NHVETHK)	0.81	240	> 5	3.6	3.6
Isolated 5V NMOS with mid oxide	nmos5i, nmos5i_6, nmos5i_h_6	(MOSS, MOSSA) +ISOMOS	0.91	465	> 7	5.5	5.5
Isolated 5V PMOS with mid oxide	pmos5i	(MOSS, MOSSA) +ISOMOS	1.01	190	> 7	5.5	5.5
Isolated 5V NMOS with mid oxide (HV)	nmos5ia, nmos5ia_6	(MOSS,MOSSA) +HVMOSMID	0.88	420	> 7	5.5	5.5
Isolated 5V PMOS with mid oxide (HV)	pmos5ia	(MOSS,MOSSA) +HVMOSMID	1.10	175	> 7	5.5	5.5
Isolated 5V NMOS with mid oxide (HV)	nmos5ic, nmos5ic_6	(MOSS,MOSSA) +NHVEMID	0.90	465	> 7	5.5	5.5
Isolated 5V PMOS with mid oxide (HV)	pmos5ic	(MOSS,MOSSA) +NHVEMID	1.08	200	> 7	5.5	5.5

XH035 DEPLETION TRANSISTORS								
Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	RON [$\text{k}\Omega\cdot\mu\text{m}$]	BVDSS [V]	Max. VDS [V]	Max. VGS [V]
5V depletion NMOS with thick oxide	nmvd	DEPL	0.70	215		> 8	5.5	5.5
45V drain depl. NMOS	nhvd	DEPL	1.2	400	12	> 50	45	18
45V drain & source depletion NMOS	nhhvd	DEPL	1.1	180	31	-	45	18
90V concentric NDMOS (ESD Pwell, thick ox)	nddhg1	DEPL +NHVETHK	-	-	-	-	90 (100*)	-

Active Devices (Continued)

XH035 MEDIUM VOLTAGE TRANSISTORS									
Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	RON [$\text{k}\Omega\cdot\mu\text{m}$]	RON*A [$\text{m}\Omega\cdot\text{mm}^2$]	BVDSS [V]	Max. VDS [V]	Max. VGS [V]
10V drain NMOS	nge	NMVMOS	1.10	485	5	-	> 14	10	18
10V drain PMOS	pge	PMVMOS	0.98	183	25	-	> 14	10	18
10V d&s NMOS	ngee	NMVMOS	0.93	420	7	-	> 14	10	18
10V d&s PMOS	pgee	PMVMOS	0.92	146	32	-	> 14	10	18
12V drain NMOS	nha	MOS	0.59	97	17	-	> 13.2	12	3.6
14V drain NMOS	nmvb	THKOX	0.97	340	9	-	> 20	14	18
14V drain PMOS	pmvb	THKOX	1.01	175	30	-	> 20	14	18
14V d&s NMOS	nmmvb	(MOS, MOSLT) +THKOX	0.92	300	11	-	> 20	14	18
		MOSLL+THKOX		320	10				
14V dr&s PMOS	pmmvb	THKOX	0.95	170	30	135	> 20	14	18
14V graded NMOS	ngmmv	NMVMOS	1.00	270	13	-	> 20	14	14
14V graded PMOS	pgmmv	PMVMOS	0.95	135	40	-	> 20	14	14
18V drain NMOS	nmva	(MOS, MOSLL) +THKOX	0.95	280	13	-	> 20	18	18
		MOSLT+THKOX	0.94						
18V drain PMOS	pmva	THKOX	1.00	185	30	-	> 20	18	18
18V d&s NMOS	nmmva	MOS+THKOX	0.94	250	15	-	> 20	18	18
		MOSLL+THKOX	0.93		14				
		MOSLT+THKOX	0.92		15				
	nmmva	MOSLT+THKOX	1.00	250	14	-	> 20	18	18
18V d&s PMOS	pmmva	THKOX	1.00	150	36	-	> 20	18	18
20V compact ND-MOS (thick oxide)	ndhi	HVMOSTHK	1.30	420	9	47	> 30	20	18

XH035 HIGH VOLTAGE TRANSISTORS									
Device	Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	RON [$\text{k}\Omega\cdot\mu\text{m}$]	RON*A [$\text{m}\Omega\cdot\text{mm}^2$]	BVDSS [V]	Max. VDS [V]	Max. VGS [V]
45V drain NMOS	nhv	THKOX	0.90	320	15	-	> 50	45	18
45V drain PMOS	phv	THKOX	0.88	140	55	-	> 50	45	18
45V d. & s. NMOS	nhhv	THKOX	0.97	155	33	-	-	45	18
45V d. & s. PMOS	phhv	THKOX	0.97	54	130	-	-	45	18
45V NDMOS (thick oxide)	ndh	MOS+THKOX +ISOMOS	1.40	240	19.5	-	> 50	45	18
45V NDMOS (thin oxide)	ndha	MOS+THKOX +ISOMOS	0.55	150	22	-	> 50	45	3.6
45V drain compact PMOS (mid oxide)	phva	HVMOSMID	1.00	110	47	336	> 55	45 (55*)	5.5
40V compact ND-MOS (mid oxide)	ndhb	HVMOSMID	0.90	260	15	98	> 51	40	5.5
45V drain compact PMOS (thick oxide)	phvb	HVMOSTHK	1.35	190	42.6	305	> 55	45 (55*)	18

* value @ Tj=-25°C ... +85°C

Active Devices (Continued)

XH035 HIGH VOLTAGE TRANSISTORS (CONTINUED)									
Device	Name	Available with module	VT [V]	IDS [μ A/ μ m]	RON [k Ω · μ m]	RON*A [m Ω ·mm ²]	BVDSS [V]	Max. VDS [V]	Max. VGS [V]
45V compact NDMOS (thick oxide)	ndhc	HVMOSTHK	1.35	335	14	92	>58	45 (55*)	18
70V drain PMOS (mid oxide)	phvc	HVMOSMID	1.12	85	62	524	> 85	70 (75*)	5.5
70V NDMOS (mid ox)	ndhd	HVMOSMID	0.88	245	20	171	> 88	70 (75*)	5.5
70V drain PMOS (thick oxide)	phvd	HVMOSTHK	1.62	155	56	473	> 85	70 (75*)	18
70V NDMOS (thick oxide)	ndhe	HVMOSTHK	1.33	310	18	154	> 88	70 (75*)	18
90V drain PMOS (mid oxide)	phve	HVMOSMID	1.12	85	72	716	> 102	90 (100*)	5.5
90V NDMOS (mid oxide)	ndhf	HVMOSMID	0.83	245	21	201	> 110	90 (100*)	5.5
90V drain PMOS (thick oxide)	phvf	HVMOSTHK	1.60	150	66	657	> 105	90 (100*)	18
90V NDMOS (thick oxide)	ndhg	HVMOSTHK	1.33	310	19	181	> 110	90 (100*)	18
40V concentric NDMOS (ESD Pwell, mid oxide)	ndhb1	NHVEMID	0.79	175	23	151	> 51	40	5.5
45V concentric NDMOS (ESD Pwell, thick oxide)	ndhc1	NHVETHK	1.25	230	19	124	> 58	45 (55*)	18
70V concentric NDMOS (ESD Pwell, mid oxide)	ndhd1	NHVEMID	0.78	173	27	231	> 81	70 (75*)	5.5
70V concentric NDMOS (ESD Pwell, thick oxide)	ndhe1	NHVETHK	1.40	185	26	222	> 88	70 (75*)	18
90V concentric NDMOS (ESD Pwell, mid oxide)	ndhf1	NHVEMID	0.78	180	28	267	> 108	90 (100*)	5.5
90V concentric NDMOS (ESD Pwell, thick oxide)	ndhg1	NHVETHK	1.38	190	27	258	> 110	90 (100*)	18
55V drain NMOS (ESD Pwell, mid ox.)	nhvb1	NHVEMID	0.76	130	25	186	> 62	55	5.5
55V drain NMOS (ESD Pwell, thick ox)	nhvc1	NHVETHK	1.65	200	19	142	> 62	55	18
75V drain NMOS (ESD Pwell, mid ox.)	nhvd1	NHVEMID	0.81	125	30	284	> 88	75	5.5
75V drain NMOS (ESD Pwell, thick ox)	nhve1	NHVETHK	1.72	190	24	227	> 88	75	18
100V drain NMOS (ESD Pwell, mid ox.)	nhvf1	NHVEMID	0.83	125	32	334	> 110	100	5.5
100V drain NMOS (ESD Pwell, thick ox)	nhvg1	NHVETHK	1.80	195	25	261	> 110	100	18

* value @ Tj=-25°C ... +85°C

Active Devices (Continued)

XH035 BIPOLAR TRANSISTORS								
Device	Name	Available	BETA	VA [V]	BVCEO [V]	VBE [mV]	max. VCE [V]	Ft max. [GHz]
Vertical PNP 8/155/12.5/100 μm^2 emitter	qp1/2/3/4	MOS, MOS5, MOSLL, MOSLT	4.5 7	190 200	-	720 735	3.6	-
Lateral PNP	qpa	MOS, MOSLL, MOSLT	27 6	4.2 14	-	730 750	3.6	-
Vertical PNP (Pwell emitter)	qpvh	MOS+THKOX, (MOSLL, MOSLT) +THKOX	45 68	>70	> 110	695	100	-
Vertical PNP (deep Pwell emitter)	qpvha	MOS+THKOX, (MOSLL, MOSLT) +THKOX	90 125	> 20	> 50	658	45	-
Isolated vertical NPN	qnva*	THKOX	46	38	> 7	680	5.5	2.9
Isolated vertical NPN (LDDNwell collector)	qnvb	(MOS, MOSLL, MOSLT) +ISOMOS	35	90	> 43	685	5.5	2.0
Isolated vertical NPN (LDDNwell collector)	qnvc	(MOS+MOS5A, MOS5) +ISOMOS	55	55	> 41	680	5.5	2.0
ESD protected HV PNP	qvhscr	PHVEMID, PHVETHK	2.3	-	> 90	537	80	-

* qnva2, qnvara, qnvarb, qnvarc are variants of the qnva. Refer to the device models for more details

Passive Devices

XH035 POLY RESISTORS						
Device	Name	Available with module	RS [Ω/\square]	Max J/W [mA/ μm]	Temp. Coeff. [$10^{-3}/\text{K}$]	Max VTB [V]
N+ Poly	rnp1	(MOS,MOS5)+HRPOLY MOSLL, MOSLT	1,000	2	-2.9	100
P+ Poly	rpp1	(MOS, MOS5)+HRPOLY, MOSLL, MOSLT	500 320	2	-0.61 -0.18	100
Very high value Poly	rhp1	XRPOLY	10,000	-	-4.1	100
Poly1	rp1	MOS, MOS5, (MOSLL, MOSLT)+LRPOLY	45	2	0.72	100
Poly1 silicided	rsp1	MOS, MOS5, (MOSLL, MOSLT) +LRPOLY	4.5	2	3.4	100
Poly2	rp2	CAPPOLY	100	2	0.40	100
low TCR Poly2	rzp2	(MOS,MOS5) +CAPPOLY, (MOSLL, MOSLT) +CAPPOLY	200 350	2	-0.17 -0.65	100
low TCR Poly1	rpp1	MOSLL, MOSLT	320	2	-0.18	100

Passive Devices (Continued)

XH035 DIFFUSION RESISTORS						
Device	Name	Available with module	RS [Ω/\square]	Thickness/junc. depth [μm]	Temp. Coeff. [$10^{-3}/\text{K}$]	Max VTB [V]
N+ diffusion	rdn	MOS, MOSS, MOSLL, MOSLT	85	0.25	1.5	6
N+ diffusion (silicided)	rsn	MOS, MOSS, MOSLL, MOSLT	3.4	0.17	3.5	6
P+ diffusion	rdp	MOS, MOSS, MOSLL, MOSLT	150 90	0.21	1.44	6
P+ diffusion (DW)	rdplw	(MOS, MOSS) +ISOMOS (MOSLL, MOSLT) +ISOMOS	143 90	-	1.6 1.5	6
P+ diffusion silicided	rsp	MOS (MOSLL, MOSLT)+ISOMOS	3.4	0.21	3.7	6
N-well	rw	MOS, MOSS, MOSLL, MOSLT	1160	1.1	3.9	6
Deep N-well	rhw	THKOX	1300	4.3	6.1	45
N+ diffusion (DW)	rdnlw	ISOMOS	85	-	1.6	6

XH035 METAL RESISTORS							
Device	Name	Available with module	RS [Ω/\square]	Thickness/junc. depth [μm]	Max J/W [$\text{mA}/\mu\text{m}$]	Temp. Coeff. [$10^{-3}/\text{K}$]	Max VTB [V]
Metal 1	rm1	MOS, MOSS, MOSLL, MOSLT	0.090	0.58	1.0	3.4	100
Metal 2*	rm2	MOS, MOSS, MOSLL, MOSLT	0.090	0.58	1.0	3.4	100
Metal 2	rm2t	METAL2	0.043	1.00	1.6	3.4	100
Metal 3**	rm3t	MOS, MOSS, MOSLL, MOSLT	0.043	0.92	1.6	3.4	100
Metal 3	rm3	METAL4, THKMET	0.090	0.58	1.0	3.4	100
Thick Metal 3	rm3l	THKMET3	0.012	2.90	6	3.5	100
Metal 4	rm4	METAL4	0.043	1.00	1.6	3.4	100
Thick Metal 4	rm4l	THKMET	0.012	2.90	6	3.5	100

*) not available with METAL2
 **) not available with METAL2, THKMET3, METAL4 or THKMET module

XH035 POD CAPACITORS						
Device	Name	Available with module	Area Cap [$\text{ff}/\mu\text{m}^2$]	BV [V]	Temp Coeff. [$10^{-3}/\text{K}$]	Max. VTB [V]
Poly on diffusion	cpod	BURDIF	3.90	> 5.0	0.002	18
Poly on diffusion	cpoda	BURDIF+THKOX	3.90	> 5.0	0.002	18
Poly on diffusion (HV)	cpod_hv	BURDIF+THKOX	0.85	> 35	0.020	20
Poly on diffusion (HDW)	cpodi_hv	BURDIF+THKOX	0.85	> 35	0.020	45

XH035 PIP CAPACITORS								
Device	Name	Available with module	Area Cap [$\text{ff}/\mu\text{m}^2$]	BV[V]	Vcoeff. [ppm/V]	Vcoeff. [ppm/V^2]	Tcoeff. [$10^{-3}/\text{K}$]	Max. VTB [V]
Poly1 - Poly 2	cpp	CAPPOLY	0.85	> 26	-120	-8.1	0.023	100
Poly1 - Poly 2 (2Terminal)	cpp2	CAPPOLY	0.85	> 26	-120	-8.1	0.023	100

Passive Devices (Continued)

XH035 SANDWICH CAPACITOR				
Device	Name	Available with module	Area Cap [fF]	Max. VCC [V]
Poly1/M1/M2/M3	csandwt	MOS, MOSS, MOSLL, MOSLT	170	100
P1/M1/M2/M3 finger	csandwtf	MOS, MOSS, MOSLL, MOSLT	255	100
P1/M1/M2/TM3 finger	csandwtf1	THKMET3	200	100
Poly1/M1/M2/M3/M4	csandwtm	METAL4	294	100
Poly1/M1/M2/M3/M4L	csandwtm1	THKMET	227	45

XH035 MIM CAPACITORS							
Device	Name	Available	Area Cap [fF/μm ²]	Voltage Coeff. [ppm/V]	Temp. Coeff. [10 ⁻³ /K]	BV [V]	max. VTB [V]
MIM	cmm, cmm2	MIM	1.25	35	0.041	> 20	100
Double MIM	cdmm, cdmm2	DMIM	2.5	35	0.041	> 20	100

XH035 STACKED CAPACITORS		
Combination	Device	Name
cpp2 on cpoda	CAPPOLY BURDIF THKOX	4.6
cpp2 on cpod_hv (or cpodi_hv)	CAPPOLY BURDIF THKOX	1.6
cmm2 on cpp	MIM CAPPOLY	2.0
cdmm2 on cpp	DMIM CAPPOLY	2.6
cmm2 on cpod_hv (or cpodi_hv)	MIM BURDIF THKOX	2.0
cdmm2 on cpod_hv (or cpodi_hv)	DMIM BURDIF THKOX	2.6
cmm2 on cpp2 on cpod_hv (or cpodi_hv)	MIM CAPPOLY BURDIF THKOX	2.7
cdmm2 on cpp2 on cpod_hv (or cpodi_hv)	DMIM CAPPOLY BURDIF THKOX	3.4

XH035 MOS VARACTOR					
Device	Name	Available with module	Tuning range [%]	Q @ 1GHz	Max VGB [V]
MOS Varactor	mosvc	MOS, MOSLT, MOSLL	71 64 56	50	3.6

XH035 DIODE VARACTOR					
Device	Name	Available with module	Tuning range [%]	Q @ 1GHz	Max VCC [V]
PIN Diode Varactor	dpvc	MOS, MOSS, MOSLT, MOSLL	36 35 36	35 30 30	3.6

Passive Devices (Continued)

XH035 INDUCTORS

Device	Name	Module	No. of Turns	Outer Diameter [μm]	Inductance [nH]	Q-Factor
Asymmetric Thick Metal 4 Inductor	I09a	THKMET	6.5	280	10.2	6.4
Symmetric Thick Metal 4 Inductor	I09b	THKMET	6.5	280	9.6	5.6
Asymmetric Thick Metal 3 Inductor	I09c	THKMET3	6.5	280	9.8	5.8
Symmetric Thick Metal 3 Inductor	I09d	THKMET3	6.5	280	9.2	5.4

XH035 POLY DIODE

Device	Name	Available with module	Vforward [V]	Vreverse [V]	Max. VTB [V]
Poly diode	dpol	(MOS, MOS5)+XRPOLY, (MOSLL, MOSLT)+LRPOLY+XRPOLY	1.13	> 4	100

XH035 PROTECTION DIODES

Device	Name	Available with module	Leakage Current [fA/μm]	BV [V]	Max Ibreak-down [μA/μm]	Max VCC [V]
20V N-type Protection *	dnp20	ISOMOS	1200	25	100	30
30V N-type Protection *	dnp30	ISOMOS, THKOX	10900	34	100	38
20V P-type Protection *	dpp20	ISOMOS	3000	26	100	31
30V P-type Protection	dpp30	THKOX	3200	37	100	40

* not available with MOS5, MOSSA, HVMOSMID, NHVEMID, PHVEMID modules

XH035 SCHOTTKY DIODES

Device	Name	Available with module	Vforward [V]	Leakage Current [nA]	BV [V]	Max. VTB [V]
Schottky	ds*	MOS+ISOMOS (MOSLT, MOSLL)+ISOMOS	0.40 0.06	0.40 40	> 21	55
Schottky	dsa**	(MOSS, MOSSA)+ISOMOS	0.06	50	> 22	55
Schottky HV isolation (thick oxide)	dsb1	MOS+ISOMOS +(THKOX, HV-MOSTHK, NHVETHK)	0.04	55	> 22	100
Schottky HV isolation (mid oxide)	dsb2	MOS+ISOMOS +(MOSSA, HVMOSMID, NHVEMID)	0.04	75	> 22	100
Schottky HV isolation (thick oxide)	dsc1	NHVETHK	0.04	70	> 22	100
Schottky HV isolation (mid oxide)	dsc2	NHVEMID	0.04	75	> 22	100

* device not available with MOS5, MOSSA, HVMOSMID, NHVEMID, PHVEMID modules

** device not available with MOSLL, MOSLT

Passive Devices (Continued)

XH035 DIFFUSION DIODES						
Device	Name	Available with module	Area Cap [ff/μm ²]	BV [V]	Leakage Current [fA/μm ²]	Max VCC [V]
N+ diff. / PW	dn	MOS, MOSS, MOSLL, MOSLT	0.790	> 7	4.0 x 10 ⁻⁴	6
N+ diff. /DPW	dnds	ISOMOS, THKOX	0.530	> 7	4.0 x 10 ⁻⁴	6
P+ diff. /NW	dp	MOS, MOSS MOSLL, MOSLT	0.810 1.000	> 7	5.0 x 10 ⁻⁴	6
P+ diff. /LDDNW	dplw	ISOMOS	0.280	> 7	5.0 x 10 ⁻⁴	6
P+ diff. /HDDNW	dphw	THKOX	0.360	> 7	5.0 x 10 ⁻⁴	6
NW /Psub (max 6V)	dw	MOS, MOSS, MOSLT, MOSLL	0.120	> 7	4.0 x 10 ⁻⁴	6
NW /Psub	dwh	MOS, MOSS, MOSLT, MOSLL	0.120	> 20	4.0 x 10 ⁻⁴	18
NW /DPW	dwds	ISOMOS, THKOX	0.390	> 21	2.0 x 10 ⁻⁴	18
PW /LDDNW (max 10V)	dwplw	ISOMOS	0.240	> 12	2.0 x 10 ⁻⁴	10
PW /LDDNW	dwplwh	ISOMOS	0.240	> 45	2.0 x 10 ⁻⁴	40
PW /HDDNW	dwphw	THKOX	0.300	> 30	3.0 x 10 ⁻⁴	30
DPW /HDDNW	ddshw	THKOX	0.190	> 50	3.0 x 10 ⁻⁴	45
LDDNW /Psub (max 10V)	dlw	ISOMOS	0.064	> 12	1.0 x 10 ⁻³	10
LDDNW /Psub	dlwh	ISOMOS	0.064	> 60	1.0 x 10 ⁻³	55
LDDNW /Psub (for pmo-sib, dsb1, dsb2)	dlwhb	ISOMOS	0.064	> 105	1.0 x 10 ⁻³	100
HDDNW /Psub (max 18V)	dhw	THKOX	0.094	> 20	6.0 x 10 ⁻⁴	18
HDDNW /Psub	dwhh	THKOX	0.094	> 105	6.0 x 10 ⁻⁴	100
Graded N diff. /DPW	dgnds	NVMOS	0.440	> 21	4.0 x 10 ⁻⁴	18
Graded P diff. /DNW	dgphw	PMVOS	0.320	> 21	5.0 x 10 ⁻⁴	18
PW /VLDDNW	dwpvw	HVMOSMID, HVMOSTHK	0.250	> 50	3.0 x 10 ⁻⁴	45
PW /MDDNW	dwplw	HVMOSMID, HVMOSTHK	0.340	> 35	5.0 x 10 ⁻⁴	30
HV DPW /LDDNW	dmpplw	HVMOSMID, HVMOSTHK	0.216	> 65	8.0 x 10 ⁻⁴	55
HV DPW /VLDDNW (max 45V)	dmpvw	HVMOSMID, HVMOSTHK	0.216	> 45	6.0 x 10 ⁻⁴	35
HV DPW /VLDDNW	dmpvwh	HVMOSMID, HVMOSTHK	0.216	> 85	6.0 x 10 ⁻⁴	75
HV DPW /MDDNW	dmpplw	HVMOSMID, HVMOSTHK	0.330	> 35	7.0 x 10 ⁻⁴	30
MDDNW /Psub	dlw	HVMOSMID, HVMOSTHK	0.140	> 110	2.0 x 10 ⁻⁴	100
VLDDNW /Psub	dvw	HVMOSMID, HVMOSTHK	0.130	> 110	2.0 x 10 ⁻⁴	100
ESD DNW /Psub	dclw	NHVEMID, NHVETHK	0.09	> 110	3.0 x 10 ⁻³	100
PW /ESD DNW	ddsclw	NHVEMID, NHVETHK	0.18	> 110	3.5 x 10 ⁻³	100
ESD PW /ESD DNW	depclw	NHVEMID, NHVETHK	0.30	> 22	2.5 x 10 ⁻³	18
DPW & ESD PW / ESD DPW	dsepclw	NHVEMID, NHVETHK	0.19	> 110	3.0 x 10 ⁻³	100
PW /ESD DNW	dwplw	NHVEMID, NHVETHK	0.30	> 25	5.0 x 10 ⁻⁴	18
HV DPW /ESD DNW	dmpclw	PHVEMID, PHVETHK	0.23	> 37	4.8 x 10 ⁻⁴	25
HV DPW /CW	dmpcw	PHVEMID, PHVETHK	0.22	> 37	4.5 x 10 ⁻⁴	25

Passive Devices (Continued)

XH035 DIFFUSION DIODES		
Device	Name	Available with module
Drain /bulk for ndhb, ndhc	dwpndh1 *	HVMOSMID, HVMOSTHK
Drain /bulk for ndhd, ndhe	dwpndh2 *	HVMOSMID, HVMOSTHK
Drain /bulk for ndhf, ndhg	dwpndh3 *	HVMOSMID, HVMOSTHK
Drain /bulk for phva, phvb	dmpphv1 *	HVMOSMID, HVMOSTHK
Drain /bulk for phvc, phvd	dmpphv2 *	HVMOSMID, HVMOSTHK
Drain /bulk for phve, phvbf	dmpphv3 *	HVMOSMID, HVMOSTHK
Drain /bulk for nhvb1, nhvc1	dlwnhv1 *	NHVMID, NHVETHK
Drain /bulk for nhvd1, nhve1	dlwnhv2 *	NHVMID, NHVETHK
Drain /bulk for nhvf1, nhvg1	dlwnhv3 *	NHVMID, NHVETHK
Drain /bulk for ndhb1	ddsndh1 *	NHVMID
Drain /bulk for ndhc1	depndh1 *	NHVETHK
Drain /bulk for nddhg1	depndh3 *	NHVETHK+ DEPL
Drain /bulk for ndhd1, ndhe1	ddsndh2 *	NHVMID, NHVETHK
Drain /bulk for ndhf1, ndgh1	ddsndh3 *	NHVMID, NHVETHK

* This device can only be used as a diode of the transistor device noted in the description

XH035 ESD PROTECTION DEVICES		
Device	Name	Available with module
PDIFF drain ballast resistor of ESD pmos, pmos5	rdp_io	MOS, MOSS, MOSLL, MOSLT
PDIFF drain ballast resistor of ESD pmv	rdpmv_io	THKOX
PDIFF drain ballast resistor of ESD pmosi, pmosia, pmosic, pmos5i, pmos5ia, pmos5ic	rdplw_io	(MOS, MOSS)+ISOMOS (MOSLT, MOSLL)+ISOMOS
NDIFF drain ballast resistor of ESD nmos, nmos5	rdn_io	MOS, MOSS, MOSLL, MOSLT
NDIFF drain ballast resistor of ESD nmv	rdnmv_io	THKOX
NDIFF drain ballast resistor of ESD nmv with drain PWELL	rdnmvwp_io	THKOX
NDIFF drain ballast resistor of ESD nmv with drain ESDPWELL	rdnmvwp_io	NHVMID, NHVETHK
NDIFF drain ballast resistor of ESD nmos, nmos5, nmosic, nmos5ic, with drain ESDPWELL	rdnep_io	NHVMID, NHVETHK
NDIFF drain ballast resistor of ESD nmosi, nmosia, nmosic, nmos5i, nmos5ia, nmos5ic	rdnlw_io	ISOMOS
Low voltage NMOS triggered SCR diode/resistor network resistor	rw_scr	MOS, MOSS, MOSLL, MOSLT
Low voltage NMOS triggered SCR diode/resistor network diode	dp_scr	MOS, MOSS

Non-Volatile-Memory

XH035 OTP MACRO

Parameter	Value
Supply voltage VDD	2.6V ... 3.6V
Operating temperature range	-40°C to 125°C
Supply voltage for program Vpp	7.0V ... 7.5V
IO	x16 data input, x16 data output bus
Data retention	Min. 20 years 125°C
Data access time	< 100ns
Program time	60µs per word
Read current	141µW/MHz (1024x8 bits)
Standby current	< 1µA

XH035 ZENER ZAP DIODE

Device	Name	Available with module	Vzapp [V]	Izapp [mA]	Vreverse [V] (un-zap/Zapped)	Max Iread [mA]
Zener Zap	dzap, dzapa *	MOS, MOSS, MOSLT, MOSLL	6	7	4 / 0.05	0.05

* The zener zap diode, dzap/dzapa is only intended as a programmable element.

XH035 POLY FUSE

Device	Name	Available with module	Unprog. Res. [Ω]	Prog. Res. [kΩ]	Prog. Max VCC [V]	Unprog. Max VCC [V]
Poly fuse	pfuse	MOS, MOSS, MOSLT, MOSLL	< 160	> 100	3.6	0.2

XH035 EEPROM

Parameter	Core EEPROM	Tiny EEPROM	Unit
Power supply in all modes	2.0 ... 3.6	1.8 ... 3.6	V
Data access time	< 100	< 250 @ VDD ≥ 2.0V	ns
Erase/Write pulse width	4 ... 8	4 ... 8	ms
Data retention	> 10 @ 85°C	> 10 @ 85°C	years
Number of erase/write Cycles @25°C	1x10 ⁵	1x10 ⁵	
Number of erase/write cycles @125°C	1x10 ⁴	1x10 ⁴	
Temperature range	-40 ... 125	-40 ... 125	°C

XH035 NVLATCH

Parameter	0.35µm NV-Latch macro
Process	Single poly logic process
Supply voltage VDD	1.8V to 3.6V
Operating temperature range	-40°C to 125°C
Configuration	up to 32 bits
Data retention	Min. 10 years @ 85°C
Product endurance	min. 10K cycles @ 125°C

STANDARD CELLS & I/O LIBRARIES

XH035 STD CELLS LIB			
Device	Library feature	Voltage range	Application benefits
D_CELLS	Standard	1.2V (LV)/2.2V/3.3V	High speed
D_CELLSL	Low power	1.2V (LV)/2.2V/3.3V	Min. area, low power consumption
D_CELLSL_5V	Low power, 5V	3.3V/5.0V	5V Power supply, low power consumption
D_CELLS_B	Standard, low noise	1.2V (LV)/2.2V/3.3V	High speed, low noise
D_CELLSL_HD	Low power, high density	1.2V (LV)/2.2V/3.3V	Min. area, low power consumption
D_CELLSL_HDJI	Low power, high density, junction isolated	1.2V (LV)/2.2V/3.3V	Min. area, low power consumption, min. noise, voltage shifting
D_CELLSL_HDM5V	Low power, 5V, multivoltage	3.3V...5.0V	Low power consumption, 5V supply, multiple voltage
D_CELLSL_JI5V	Low power, 5V, junction isolated	3.3V/5.0V	Low power consumption, junction isolated, voltage shifting, 5V supply, mid gate oxide
D_CELLSL_JI5V_100V	Low power, 5V, junction isolated	3.3V/5.0V	Low power consumption, junction isolated, 5V supply, mid gate oxide, voltage shifting up to 100V
D_CELLSL_LL	Low leakage, low power	2.2V/3.3V	Low power consumption, min. leakage
D_CELLSL_B	Low power, low noise	1.2V (LV)/2.2V/3.3V	Min. noise, low power consumption
D_CELLS_THKOX_5V	Thick gate oxide, 5V	3.3V/5.0V	High speed, thick gate oxide, 5V supply

XH035 I/O CELLS					
Device	Library Feature	V _{CORE} *	V _{IO} *	ESD Level	Application benefits
IO_CELLS	Standard, V _{CORE} = V _{IO} single supply voltage	3.3V	3.3V	4kV HBM	Pad limited
IO_CELLS_F	Standard, V _{CORE} = V _{IO} single supply voltage	3.3V	3.3V	2kV HBM	Core limited
IO_CELLS_5V	Standard, V _{CORE} ≤ V _{IO} multi supply voltage	3.3V 3.3V 5.0V	3.3V 5.0V 5.0V	4kV HBM	Pad limited
IO_CELLS_F5V	Standard, V _{CORE} ≤ V _{IO} multi supply voltage	3.3V 3.3V 5.0V	3.3V 5.0V 5.0V	2kV HBM	Core limited
IO_CELLS_N5V	Standard, V _{CORE} ≤ V _{IO} multi supply voltage, ESD improved 5V nmos	3.3V 3.3V 5.0V	3.3V 5.0V 5.0V	4kV HBM	Pad limited
IO_CELLS_FN5V	Standard, V _{CORE} ≤ V _{IO} multi supply voltage, ESD improved 5V nmos	3.3V 3.3V 5.0V	3.3V 5.0V 5.0V	4kV HBM	Core limited
IO_CELLS_MV	Standard, 2.2V/3.3V multi supply voltage	2.2V	3.3V	4kV HBM	Pad limited
IO_CELLS_MVF	Standard, 2.2V/3.3V multi supply voltage	2.2V	3.3V	2kV HBM	Core limited
IO_CELLS_FE	Standard, V _{CORE} ≤ V _{IO} multi supply voltage	3.3V 2.2V 2.2V	3.3V 3.3V 2.2V	4kV HBM	Core limited
IO_CELLS_JI3V	Junction isolated, V _{CORE} ≤ V _{IO} multi supply voltage	3.3V 2.2V 2.2V	3.3V 3.3V 2.2V	4kV HBM	Pad limited

* Please refer to the library databook for details about available PVT ranges

ANALOG LIBRARIES

XH035 OPERATIONAL AMPLIFIERS

Name	VOL [V]	VOH [V]	VICR [V]	VIO [mV]	AVD [dB]	B1 [kHz]	SR [V/μs]	PHM [°]	IDD [μA]	max. Load	Required modules
aopac01	0.25	V _{DD} -0.15	0.9 ... V _{DD} -0.40	< 5	90	2600	2.0/2.0	75	325	50pF/50kΩ	MOS
aopac02	0.15	V _{DD} -0.25	-0.10 ... V _{DD} -1.25	< 5	96	2200	2.3/2.3	75	290	50pF/50kΩ	MOS
aopac03	0.1	V _{DD} -0.10	-0.3 ... V _{DD} +0.3	< 10	110	2000	2.0/2.0	75	300	50pF/50kΩ	MOS
aopac04	0.2	V _{DD} -0.25	-0.5 ... V _{DD} +0.3	< 12	105	1900	1.7/1.8	75	190	50pF/50kΩ	MOS
aopac05	0.20	V _{DD} -0.20	-0.3 ... V _{DD} -1.05	< 15	98	68	0.04/0.04	70	10	30pF/750kΩ	MOS
aopac06	0.16	V _{DD} -0.50	0.90 ... V _{DD} -0.60	< 8	90	9400	9.7/8.8	70	680	30pF/10kΩ	MOS
aopac08	0.92	V _{DD} -0.20	0.80 ... V _{DD} -0.40	< 5	90	2900	1.9/1.9	65	140	25pF/30kΩ	MOS
aopac12	0.16	V _{DD} -0.37	0 ... V _{DD} - 1.5	< 14	90	2250	1.3/1.15	76	545	30pF/50kΩ	MOS, CAP-POLY
aopac13	0.2	V _{DD} -1.11	0.02 ... V _{DD} -1.2	< 5	100	1800	1.7/1.7	62	90	30pF/ 1000kΩ	MOS, BURDIF, THKOX
aopac01ji	0.12	V _{DD} -0.2	-0.3 ... V _{DD} -1.2	<10	110	1790	0.9/1.0	87	45	20pF/50kΩ	MOS, ISOMOS, MIM, HRPOLY

Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ... 85°C, all Opamps feature a standby mode

XH035 COMPARATORS

Name	VICR [V]	TPD for 50mV Overdrive [ns] L->H/H->L	Conditions C _L [pF]; R _L [kΩ]	Input Offset Voltage [mV]	Supply Current [μA]	Required modules
acmpc01	0.05...VDD-1.65	525/550	1;1000	< 10	2	MOS
acmpc02	0.9...VDD-0.3	800/730	1;1000	< 5	2	MOS
acmpc03	-0.3...VDD+0.3	120/130	1;1000	< 10	25	MOS
acmpc04	0...VDD+0.3	110/115	1;1000	< 10	8	MOS
acmpcn01ji	0.9...VDD-0.30	500/285	0.1; no dc	< 5	3	MOS, ISOMOS
acmpcp01ji	0.1...VDD-1.2	220/780	0.1; no dc	< 5	3	MOS, ISOMOS

Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ... 85°C, all Comparators feature a standby mode

XH035 LOW VOLTAGE BANDGAP

Name	Bandgap Voltage (unloaded) [V]; T = 30°C	Temperature Coefficient [ppm/°C]	Supply Voltage [V]	Supply Current [μA]	Required Module
abgpc 07	1.285	±300; T= -40 °C to T= 125°C	2.2 ... 3.6	45.0@VDD=3.3V	MOS
abgpc08	1.280	±200; T= -40 °C to T= 125°C	2.2 ... 3.6	35.0@VDD=3.3V	MOS, BURDIF, THKOX
abgpc09	1.280	±200; T= -40 °C to T= 125°C	2.1 ... 3.6	40.0@VDD=3.3V	MOS
abgpc11	1.285	±200; T= -40 °C to T= 125°C	1.8 ... 3.6	40.0@VDD=3.3V	MOS

Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ... 125°C, all Bandgaps feature a standby mode

ANALOG LIBRARIES (Continued)

XH035 BANDGAPS				
Name	Bandgap Voltage (unloaded) [V]	Temperature Coeff. [ppm/°C]	Supply Current [µA]	Required Module
abgpc01	1.265*	±250; T= -40 °C to 125°C	20	MOS
abgpc02	1.225*	±150; T= -40 °C to 125°C	44	MOS, CAPPOLY
abgpc04	1.280*	±200; T= -40 °C to 125°C	50	MOS, CAPPOLY
abgpc01ji	1.207*	±100; T= -40 °C to 125°C	18	MOS, ISOMOS, MIM, HRPOLY

* @T=27°C, Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ... 125°C, all Bandgaps feature a standby mode

XH035 POWER ON RESET				
Name	High Treshold Voltage /Low Treshold Voltage[V]	Delay VDD->H to POR->L TDEL [µs]	DC-Current POR IDDL [µA]	Required Module
aporc01	1.95	12	-	MOS
aporc02	2.04 /1.80	7.5	2	MOS
aporc03	1.95	7.5	1.5	MOS

Note: All Parameters are valid for VDD: 2.7V to 3.6V, T: -40 ...85°C

XH035 CRYSTAL OSCILLATORS				
Name	Frequency [kHz]	Conditions	Supply Current (specified @ VDD=5V, T=25°C) [µA]	Required Module
axtoc01	1000 ... 6000	@VDD=3.3V to 5.5V; T=25°C	110, F=2MHz	MOS, CAPPOLY
axtoc02	32.768	@VDD=3.3V to 5.5V; T=25°C	40	MOS, CAPPOLY

Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ...85°C

XH035 RC OSCILLATORS				
Name	Frequency [kHz]	Conditions	Supply Current (specified @ VDD=3.3V, T=25°C) [µA]	Required Module
arcoc01	13	@VDD=3.3V; T=25°C	3.5	MOS
arcoc02	200	@VDD=3.3V; T=25°C	22	MOS, CAPPOLY
arcoc03	970	@VDD=3.3V; T=25°C	45	MOS, CAPPOLY
arcoc04	136 / 200 / 390	@VDD=3.3V; T=25°C dig. code= 0h / 10h / 1Fh	22	MOS, CAPPOLY
arcoc05	650 / 970 / 1820	@VDD=3.3V; T=25°C dig. code= 0h / 10h / 1Fh	43	MOS, CAPPOLY
arcoc06	1000 ... 8000	@VDD=3.3V; T=25°C IBIAS=1µA ... 10µA	60 @ I _{BIAS} =8µA	MOS, CAPPOLY
arcoc08	850	@VDD=3.3V; T=25°C 6 trimming inputs	30	MOS, BURDIF, THKOX

Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ...125°C

ANALOG LIBRARIES (Continued)

XH035 BIAS CELLS

Name	Bias Voltage VBP for PMOS [V]	Temp. Coeff. IVBP [ppm/°C]	Bias Voltage VBN for NMOS [V]	Temp. Coeff. IVBN [ppm/°C]	Supply Current [μA]	Required Module
abiac01	VDD-1.15 ¹	-1700	0.760 ²	-1900	12	MOS
abiac02	VDD-1.15 ¹	-3900	0.765 ²	-3900	12	MOS
abiac03	VDD-0.930 ¹	2000	0.650 ²	1800	0.8	MOS

¹@VDD=3.3V, T=25°C ²@VDD=3.3V, T=30°C
 Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -4085°C, all Bias Cells feature a standby mode

XH035 BIAS CELLS 2

Name	Output Current IOUT [μA]	Temperature Coefficient IOUT [ppm/°C]	Supply Current [μA]	Required Module
acsoc01	2	-1800	9	MOS
acsoc02	2	-4200	8.5	MOS

Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -4085°C, all Bias Cells feature a standby mode

XH035 ADC

Name	Principle	Resolutions [Bits]	Accuracy [LSB] INL/DNL	Conversion Time [Clock Cycles]	Supply Current [μA]	Required Module
aadcc01	two-step	8	±1.0 / ±0.3	4	250	MOS, CAPPOLY
aadcc02	successive approximation	10	±1.0 / ±0.4	12	90	MOS, CAPPOLY

Note: All Parameters are valid for VDD: 2.7V to 3.6V, T: -4085°C

XH035 DAC

Name	Principle	Resolutions [Bits]	Accuracy [LSB] INL/DNL	Conversion Time [μs]	Ref. Voltage Range [V] min/max	Required Module
adacc02	voltage scaling	10	±1.5 / ±1	1.0*	1.2 / 3	MOS, CAPPOLY

* @ Vref=3.3V, CL=2pF
 Note: All Parameters are typical, VDD: 2.7V to 3.6V, T: -4085°C

XH035 OVER-TEMPERATURE DETECTOR

Name	Threshold Temp T _H [°C] typ	Voltage Coeff. of Threshold Temp [°C/V] VC _{TH} / VC _{TL}	Low Output Voltage [V]	High Output Voltage [V]	Supply Current [μA]	Required Module
atmpc01	140	2	VSSA	VDDA	10	MOS
atmpc02	130 @ trimming code 00	2	VSSA	VDDA	11	MOS

Note: All Parameters are valid for VDD: 2.7V to 3.6V, T: -40140°C, the temperature of 140°C has to be considered as absolute maximum ratings

XH035 UNDER-VOLTAGE DETECTOR

Name	High Threshold Voltage V _{TH} [V] typ	Low Threshold Voltage V _{TH} [V] typ	Digital Voltage Supply [V]	Auxillary Voltage Supply [V]	Supply Current [μA]	Required Module
auvdet_vdd01ji	2.1	1.88	2.2 ... 3.6	2.7 ... 3.6	10	MOS, ISOMOS, HRPOLY

Note: All Parameters are valid for VDD: 2.7V to 3.6V, T: -4085°C.

ANALOG LIBRARIES (Continued)

XH035 HV DRIVERS

Name	Load Current [mA] Max	Load Supply Voltage [V] Max	Output Resistance [Ω]	Output Surge Voltage [V]	Load Inductance [H] Max.	Required Module
adrvc02	50	15	10; VDD=3.3V, VDDAH=12V, T=25°C	0.7	0.50	MOS, THKOX
adrvc03	50	15	4; VDD=3.3V, VDDAH=12V, T=25°C	21	0.50	MOS, THKOX,

Note: All Parameters are valid for T: -40 ...85°C

XH035 HV RC OSCILLATOR

Name	Frequency [kHz]	Conditions	Supply Current (specified @ VDD=12V, T=25°C) [μ A]	Required Module
arcoc 07	430	@VDD=12V; T=25°C	170	MOS, THKOX

Note: Supply voltage: 6-15V. All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ...85°C

XH035 HV BIAS

Name	Current through VBP [μ A]; @ VDD=15V, T=25°C	Temperature Coeff. IVBP [ppm/°C]	Current through VBN [μ A]; @ VDD=15V, T=25°C	Temperature Coeff. IVBN [ppm/°C]	Supply Current [μ A]	Required Module
abiacc04	2.0	\pm 1500; T=-40°C to 85°C, VDD=12V	2.0	\pm 1500; T=-40°C to 85°C, VDD=12V	6	MOS, THKOX

Note: Supply voltage = 7 - 15V. All Parameters are typical, VDD: 2.7V to 3.6V, T: -40 ...85°C, all Bias Cells feature a standby mode

XH035 HV BANDGAP

Name	Bandgap Voltage (unloaded) [V]; T=30°C	Temperature Coeff. [ppm/°C]	Supply Current [μ A]	Supply Range [V]	Required Module
abgpc06	1.262	\pm 250; T=-40°C to 125°C	60	6 - 15	MOS, THKOX
abgpc10	1.191	\pm 200; T=-40°C to 125°C	70	3 - 5.5	MOS, THKOX, HRPOLY

Note: All parameters are typical T: -40 ...85°C, all Bandgaps feature a standby mode

XH035 HV COMPARATORS

Name	VICR [V]	TPD for 50mV Overdrive [ns] L->H/H->L	Conditions C _L [pF]; R _L [k Ω]	Input Offset Voltage [mV]	Supply Current [μ A]	Required modules
acmpc05	1.2...VDD-1.7	270/250	1.0;10000	< 10	30	MOS, THKOX

Note: All Parameters are typical, VDD: 6V to 15V, T: -40 ... 85°C, all Comparators feature a standby mode

XH035 HV OPERATIONAL AMPLIFIERS

Name	V _{OL} [V]	V _{OH} [V]	V _{ICR} [V]	V _{IO} [mV]	A _{VD} [dB]	B ₁ [kHz]	SR [V/ μ s]	PHM [°]	I _{DD} [μ A]	max. Load	Required modules
aopac11	0.4	V _{DD} -0.9	0 ... V _{DD} -1.8	< 15	100	1100	1.8/2.1	80	665	30pF/15k Ω	MOS, THKOX

Note: All Parameters are typical, VDD: 8V to 15V, T: -40 ...85°C, all Opamps feature a standby mode

XH035 HV REGULATORS

Name	Typ. Output Voltage [V]	Max Output Current [mA]	Line Regulation [mV/V]	Supply Current [μ A]	Supply Voltage [V]	Required Module
aregc01	3.30	20	1; VDDAM=4V-6V	90	4 - 5.5	MOS, THKOX
aregc02	3.30	20	0.8; VDDAH=6V-18V	310	6 - 18	MOS, THKOX, ISOMOS
aregc04	3.30	5	0.4; VDDAM=4V-5.5V	85	4 - 5.5	MOS, THKOX, HRPOLY

Note: All Parameters are valid for T: -40 ...85°C

ANALOG LIBRARIES (Continued)

XH035 RF LNA CELLS								
Name	S21 [dB]	NF [dB]	ICP1dB [dBm]	IIP3 [dBm]	ZIN [Ω]	ZOUT [Ω]	IS [mA]	Required modules
LNA1	11	2.4	-11	-2	36-j52	35-j39	8.6	MOS, HRPOLY, MIM
LNA2	14	1.8	-10	-2	31-j209	24 j0	3.3	MOS, HRPOLY MIM, THKMET

Note: All Parameters are typical, VDD: 2.5V to 3.6V, T: -4085°C, all LNA feature a standby mode

XH035 RF DIVIDER CELLS						
Name	NDIV	fIN_MAX [GHz]	PNDIV32 [dBc/Hz] foffs= 10kHz	IS [mA]	Required modules	
DIV32	32	1.7	-130	1.0	MOS, HRPOLY, MIM	

Note: All Parameters are typical, VDD: 2.5V to 3.6V, T: -4085°C, Divider feature a standby mode

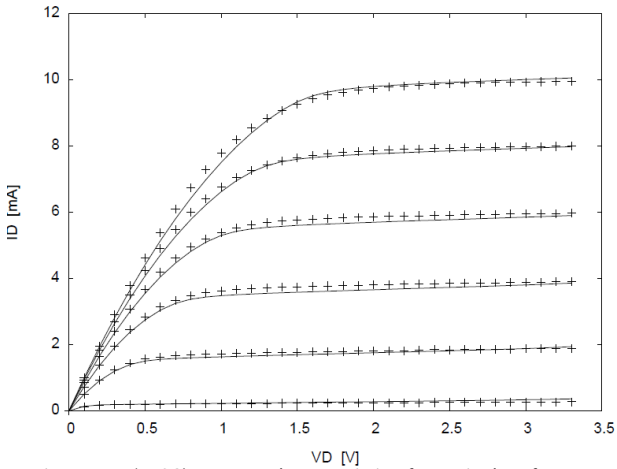
XH035 RF BIAS CELLS					
Name	Bandgap Voltage (buffered) [V]	Temperature Coefficient [ppm/C]	IPTAT [μ A]	IRZP [μ A]	Required modules
BIAS	1.22	58; T=-40 °C to T=30°C 21; T=30 °C to T=125°C	10	10	MOS, CAPPOLY, HRPOLY, MIM

Note: All Parameters are typical, VDD: 2.5V to 3.6V, T: -4085°C, Bias cell feature a standby mode

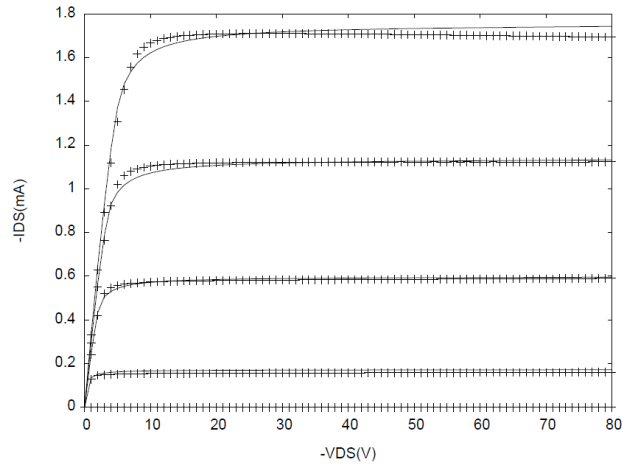
XH035 RF PADS			
Device	Library Feature	Voltage Range	Application benefits
RFPADS_M3	RF pad IO library (Metal 3)	3.3V	RF Design
RFPADS_M4	RF pad IO library (Metal 4)	3.3V	RF Design
RFPADS_ML	RF pad IO library (Power Metal)	3.3V	RF Design
RFPADS_5VM3	RF pad IO library (Metal 3)	5.0V	RF Design
RFPADS_5VM4	RF pad IO library (Metal 4)	5.0V	RF Design
RFPADS_5VML	RF pad IO library (Power Metal)	5.0V	RF Design

XH035 HV CELLS				
Device	Library Feature	Voltage Range	ESD Level	Application benefits
HV_CELLS	Special LV I/O, operating voltage specific HV ESD protection cells	LV, 12V-100V	2kV-8kV HBM	MOS, MOSLL or MOSLT Customized I/O Design
HV_CELLS_MID	Special LV I/O, operating voltage specific HV ESD protection cells	LV, 12V-100V	2kV-8kV HBM	MOS, MOSLL or MOSLT Customized I/O Design

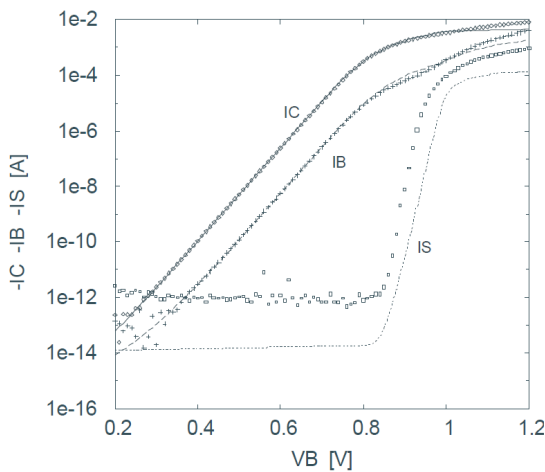
EXAMPLES FOR MEASURED AND MODELED PARAMETER CHARACTERISTICS



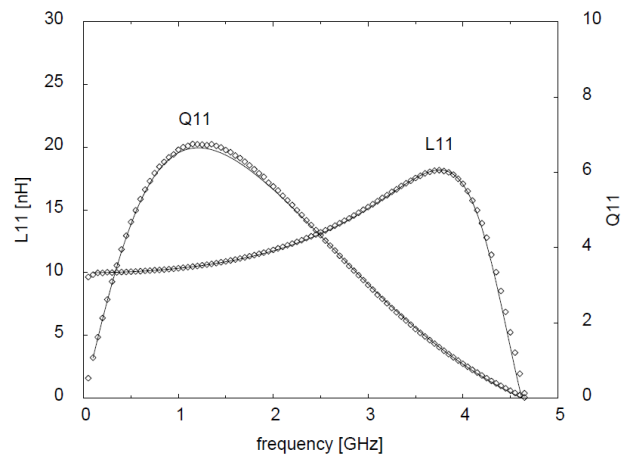
Device nmos (MOS): output characteristic of a typical wafer. W/L = 20/0.35, VGS = 0.8, 1.3, 1.8, 2.3, 2.8, 3.3V, += measured, solid line = BSIMv3 model



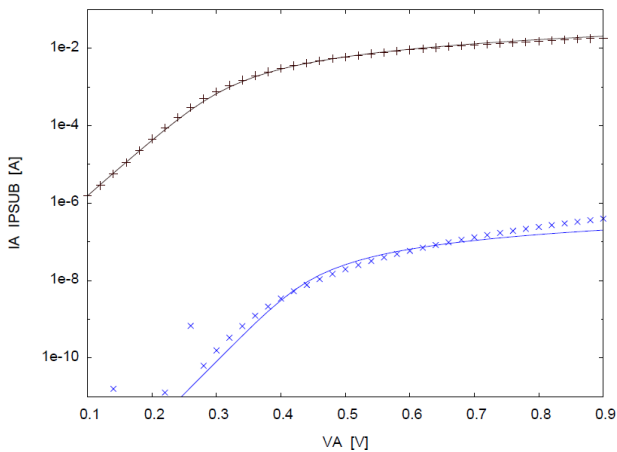
Device phvc: output characteristic of a typical wafer W/L = 20/2, -VGS = 1, 2, 3, 4, 5V, VSB = 0V, += measured, solid line = BSIM3v3_XHV model



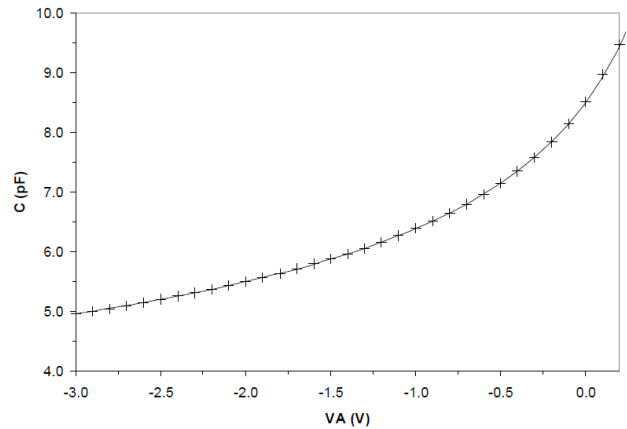
Device qnva: gummel plot of vertical NPN bipolar transistor for a typical wafer. LE = 10µm, VB = VC, VE = 0V, symbols = measured, lines = SPICE model



Device I09a: inductance and quality factor for a typical wafer symbols = measured, solid line = SPICE model

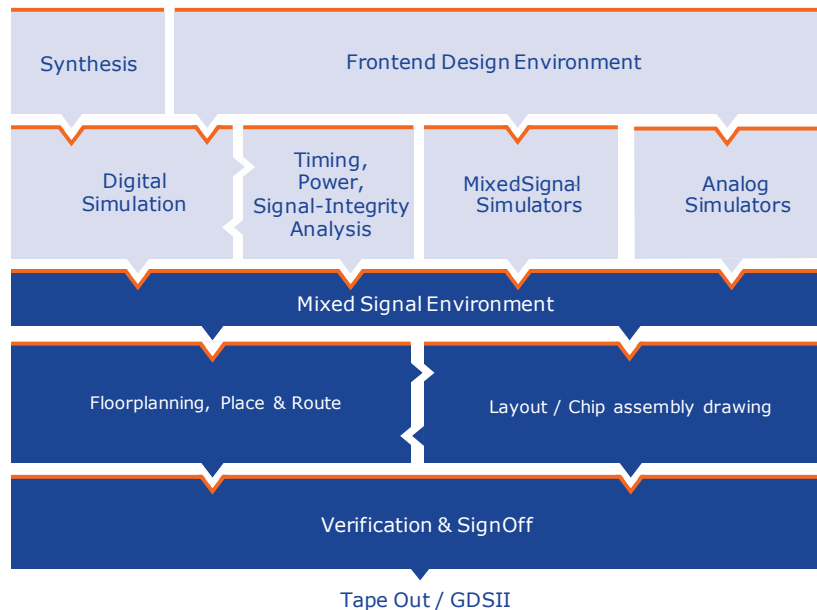


Device dsb2: diode current (black) and substrate current (blue) vs. forward voltage for a typical wafer. 2.2µm x 10.2µm x16 schottky diode. Vanode=0.1V to 0.9V, 0.02V step. symbols = measured, lines = SPICE model



Device dpvc (MOSLT): capacitance vs. anode voltage characteristic of diode varactor for a typical wafer, no. of PDIFF stripes = 168, length of PDIFF stripe = 10µm, += measured, solid line = SPECTRE model

XH035 SUPPORTED EDA TOOLS



Note: Diagram shows overview of reference flow at X-FAB. Detailed information of supported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center X-TIC.

X-FAB'S IC DEVELOPMENT KIT "THEKIT"

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which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well. The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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