

0.18 µm Process Family:

> XH018



0.18 Micron Modular Analog Mixed HV Technology

DESCRIPTION

The XH018 series is X-FAB's 0.18 micron Modular Mixed Signal HV CMOS Technology. Based upon the industrial standard single poly with up to six metal layers 0.18 micron drawn gate length N-well process, integrated with high-voltage, Non-Volatile-Memory and ultra-low noise modules, the platform is ideal for SOC applications in the automotive mar-

ket, as well as emdedded high-voltage applications in the communications, consumer and industrial market.

Comprehensive design rules, precise SPICE models, analog and digital libraries, IPs and development kits support the process for major EDA vendors.

KEY FEATURES OVERVIEW

- 0.18-micron single poly, up to six-metal N-well CMOS basic process
- Modular concept
- Up to 175°C operating temperature, extending beyond AEC Q100 requirement
- Low Power core module
- Thick metal layers optional module
- Integrated digital, analog, HV and NVM in a single process
- Isolation well for all 1.8V, 3.3V and 40V MOS devices
- 10-45V sym./asy. HVMOS transistors
- 35-45V DMOS transistors
- Vertical NPN BJT
- ESD protected HV PNP for reverse polarity protection (e.g. for LIN pins)
- **Ultra-low-noise NMOS/PMOS (3.3V) and 1.8V NMOS transistors**
- **MOS 1/f noise characterized & included in model**
- Low Vt Transistors
- High-reliability NVM using SONOS technology
- Various types of memory compiler (e.g. RAM, ROM, NVRAM, TrimOTP)
- Integrated high-ohmic poly resistor in core module (zero mask penalty)
- High capacitance single, double, triple MIM and fringe capacitors
- Characterized photo diodesUV to NIR sensible
- Schottky & protection diodes
- High density up to 125000 gates per mm²
- Typical and worst-case models (MOS, BJT, RES, CAP)
- Assura verification deck
- Common-Timing-Engine in Cadence P&R encounter platform
- Cadence & Mentor Graphic PDK

APPLICATIONS

- High temperature mixed-signal embedded systems/ system-on-chip (SOC)
- Automotive
- Analog frontends for sensors
- High precision mixed signal circuits
- Embedded high-voltage applications
- Power management IC
- Communications, Consumer and Industrial markets

QUALITY ASSURANCE

X-FAB spends a lot of effort to improve the product quality and reliability and to provide comprehensive support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by

strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, IATF 16949 and other standards.

DELIVERABLES

- PCM tested wafers
- Optional engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional design services: feasibility studies, Place & Route, synthesis, custom block development

DIGITAL LIBRARIES

- Foundry-specific optimized libraries
- Low power, low leakage library for energy efficient and small size digital blocks
- Junction isolated library for low noise applications
- Multi-voltage library for multi-voltage and power cut-off applications
- Liberty™ synthesis models
- IEEE 1364 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models

ANALOG LIBRARIES

- Operational Amplifiers
- Bias Cells
- Digital-to-Analog Converters
- Analog-to-Digital Converters
- RC Oscillators
- Power-On/Off-Reset
- Comparators
- Bandgaps
- Voltage Regulators
- Over-Temperature Detector

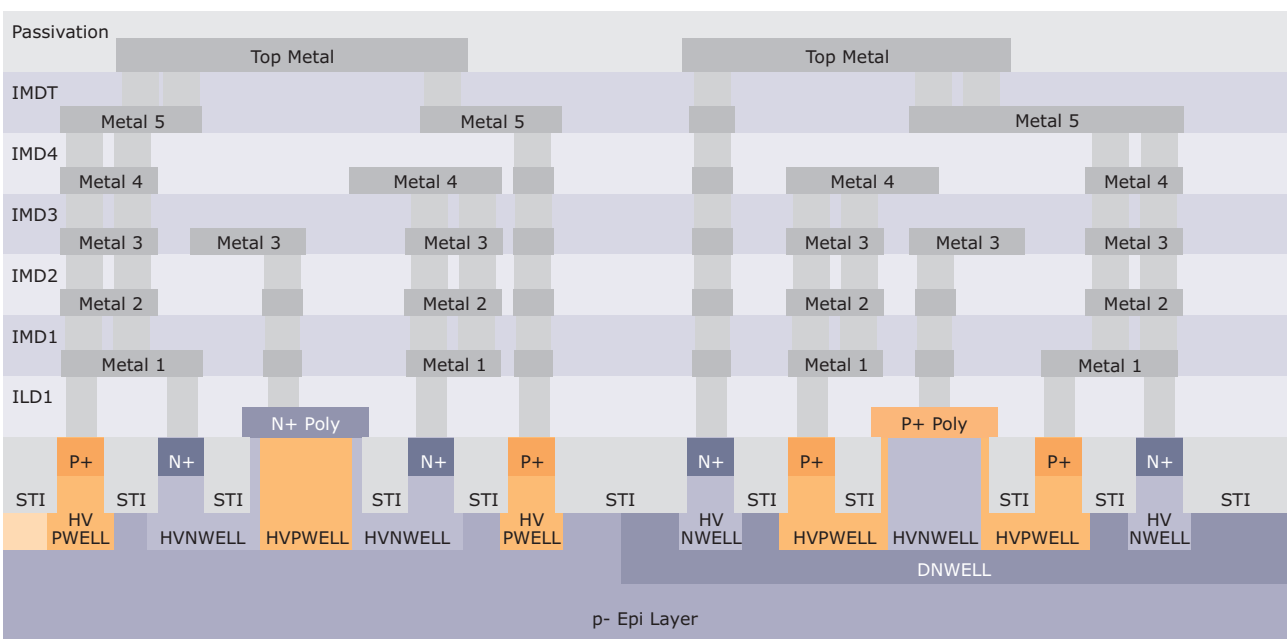
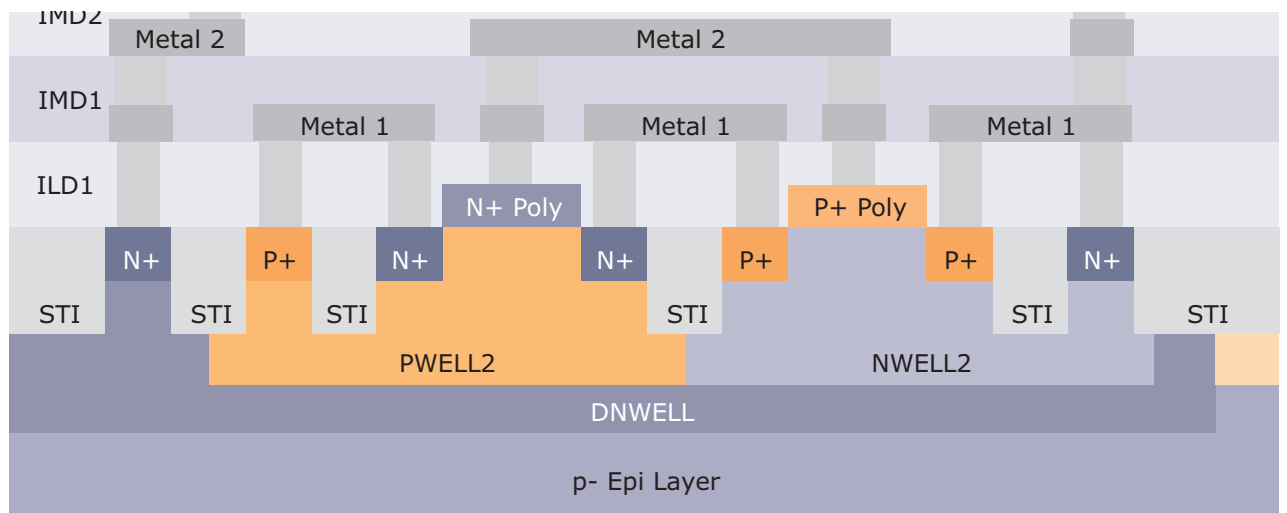
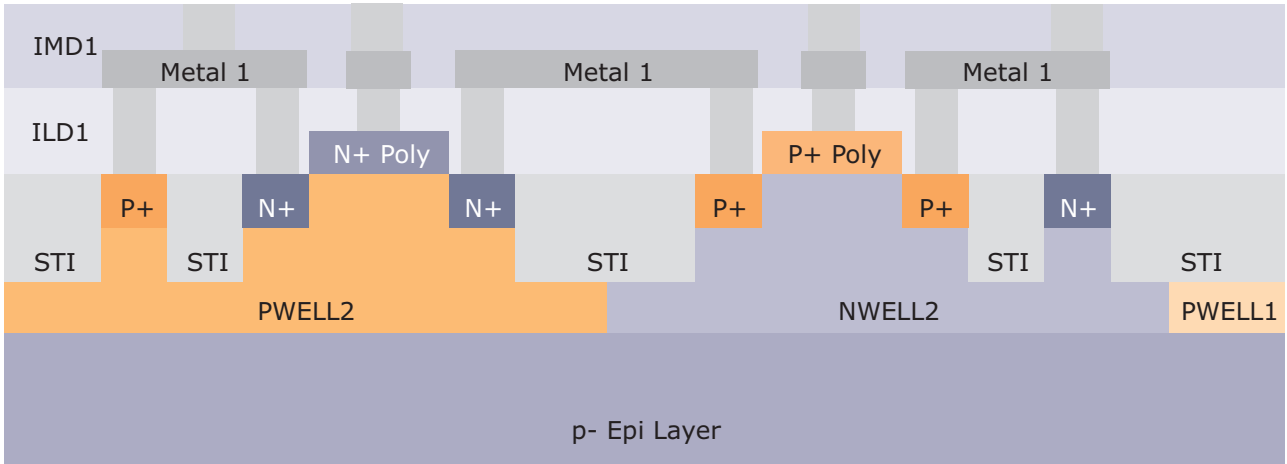
PRIMITIVE DEVICES

- (Isolated) 1.8V, 3.3V LP NMOS/PMOS
- 10V, 15V, 20V, 45V HVMOS, Sym./Asy.
- 35V, 40V, 45V lateral DMOS, isolated
- Depletion NMOS
- Bipolar transistors, ESD protected
- Sandwich, Fringe, MIM Capacitors
- Resistors
- Diffusion, Schottky, Protection, Photo Diodes

XH018 BASIC DESIGN RULES

| Mask | width [μm] | Spacing [μm] |
|-----------------------|------------|--------------|
| N-well | 0.86 | 1.4 |
| Active Area | 0.22 | 0.28 |
| Poly-silicon Gate | 0.18 | 0.25 |
| Poly-silicon Resistor | 0.44 | 0.44 |
| Contact | 0.22 | 0.25 |
| Metal 1 | 0.23 | 0.23 |
| Via 1, 2, 3, 4 | 0.26 | 0.26 |
| Metal 2, 3, 4, 5 | 0.28 | 0.28 |
| Top Via | 0.36 | 0.35 |
| Top Metal | 0.44 | 0.46 |
| Thick Metal | 3.0 | 2.5 |

XH018 DEVICES SCHEMATIC CROSS SECTION



XH018 PROCESS FLOW

| Core Modules | Additional Modules | |
|------------------------|------------------------|----------------------------------|
| Wafer Start | HV gate oxide | HVMOS |
| | Deep HV N-well | HVPMOS/ BIPESD/ SCHOTTKY |
| Active area | Deep N-well | HVMOS/ ISOMOS/ ISOMOS2/ PHOTODIO |
| | HV wells | HVMOS |
| | Shallow HV N-well | NHVE |
| | Shallow HV P-well | PHVE |
| | DMOS drift implant | DMOS |
| | Depletion implant | DEPL |
| | HV depletion implant | HVDEPL |
| | Non volatile memory | NVM/ FLASH |
| 3.3V wells | CPOD implant | CPOD |
| 1.8V wells | 1.8V low Vt wells | LVT |
| | 1.8V medium Vt wells | SVT |
| Dual gate oxide | | |
| Poly silicon gate | | |
| Source/ Drain implants | MRPOLY implant | MRPOLY |
| Salicidation | | |
| Contact | | |
| Metal 1 | | |
| Via 1 | | |
| Metal 2 | | |
| | Single MIM capacitor | MIM23/ MIMH23 |
| | Double MIM capacitor | DMIM/ DMIMH |
| | Triple MIM capacitor | TMIM/ TMIMH |
| | Via 2 | |
| | Metal 3 | MET3 |
| | Single MIM capacitor | MIM34/ MIMH34 |
| | Double MIM capacitor | DMIM/ DMIMH |
| | Triple MIM capacitor | TMIM/ TMIMH |
| | Via 3 | |
| | Metal 4 | MET4 |
| | Triple MIM capacitor | TMIM/ TMIMH |
| | Via 4 | |
| | Metal 5 | MET5 |
| | MIM capacitor | MIM/ MIMH |
| | Top Via | METMID |
| | Top Metal | |
| | Thick Via | METTHK |
| | Thick Metal | |
| | Planarized passivation | FLATPV |
| | Planarized passivation | SFALTPV |
| PAD | Polyimide | PIMIDE |
| | | mask steps |

XH018 CORE MODULE

| Module Name | Descriptions | Masks No. |
|-------------|---------------------------------------|-----------|
| LPMOS | Low power 1.8V, 3.3V CMOS CORE module | 19 |

XH018 ADDITIONAL MODULES

| | | |
|----------|---|-----|
| CPOD | POD capacitor module | 1 |
| CPODHV | HV POD module | 2 * |
| MRPOLY | Medium resistance polysilicon module | 1 |
| ISOMOS | Triple well (DNWELL) isolated CMOS module | 1 |
| ISOMOS2 | Triple well (DNWELLMV) isolated CMOS module | 1 |
| HIGHTEMP | High temperature module | 0 |
| LVT | 1.8V low Vt module | 2 |
| SVT | 1.8V medium Vt module | 2 |
| LNPMOS3 | 3.3V low noise PMOS module | 1 |
| ULN | Low noise CMOS module | 1 |
| DEPL | Depletion module | 1 |
| HVDEPL | High voltage depletion module | 1 |
| DMOS | DMOS module | 1 |
| HVMOS | High voltage module | 5 * |
| HVNMOS | HVNMOS module | 3 * |
| NHVE | High voltage extension module | 1 |
| HVPMOS | HVPMOS module | 6 * |
| PHVE | High voltage extension module | 1 |
| SCHOTTKY | Schottky module | 2 * |
| MIM | MIM capacitor module | 1 |
| MIM23 | Metal2-Metal3 MIM capacitor module | 1 |
| MIM34 | Metal3-Metal4 MIM capacitor module | 1 |
| DMIM | Double MIM capacitor module | 1 |
| TMIM | Triple MIM capacitor module | 1 |
| MIMH | Single high capacitance MIM capacitor module | 1 |
| MIMH23 | Metal2-Metal3 high capacitance MIM capacitor module | 1 |
| MIMH34 | Metal3-Metal4 high capacitance MIM capacitor module | 1 |
| DMIMH | Double high capacitance MIM capacitor module | 1 |
| TMIMH | Triple high capacitance MIM capacitor module | 1 |
| NVM | Non-volatile-memory module | 2 |
| FLASH | Flash memory module | 0 |
| OTP3 | One-Time Programmable memory module | 0 |
| ANODOP | UV diode module - anode | 1 |
| CATDOP | UV diode module - cathode | 1 |
| UVWINDOW | UV diode module - UV window | 0 |

* These modules might have different mask count when in combination with other modules, as listed in the table "XH018 Additional Mask Count for Module Combination".

| XH018 ADDITIONAL MODULES (CONT') | | |
|----------------------------------|-------------------------|-----|
| BIPESD | ESD module | 3 * |
| ESDPNP | ESD module | 5 * |
| FLATPV | Flat passivation module | 0 |
| SFLATPV | Sensor flat passivation | 0 |
| PHOTODIO | Photo diode module | 0 |
| MET3 | 3-metal module | 2 |
| MET4 | 4-metal module | 2 |
| MET5 | 5-metal module | 2 |
| METMID | Top metal module | 2 |
| METTHK | Thick metal module | 2 |
| PIMIDE | Polyimide module | 1 |

| XH018 ADDITIONAL MASK COUNT FOR MODULE COMBINATION | | |
|--|-------------------------------|--------------------------------|
| Module Name | When combines with modules | Combined additional mask count |
| CPODHV | HVMOS/ HVNMOS/ HVPMOS/ ESDPNP | 0 |
| HVMOS | ISOMOS/ ISOMOS2 | 5 |
| HVNMOS | HVMOS | 5 |
| HVNMOS | HVPMOS | 6 |
| HVNMOS | HVPMOS+HVNE | 6 |
| HVPMOS | HVMOS | 7 |
| HVPMOS | HVNMOS+PHVE | 7 |
| BIPESD | HVMOS | 7 |
| ESDPNP | HVPMOS | 6 |
| SCHOTTKY | HVMOS | 6 |
| SCHOTTKY | HVNMOS | 4 |
| SCHOTTKY | HVPMOS | 6 |

| XH018 RESTRICTION FOR MODULE COMBINATIONS | | |
|---|--|--|
| Module name | Use of the module also requires use of the following module(s) | Use of the module is not available with the use of the following module(s) |
| LPMOS | MET3+METMID | |
| CPODHV | CPOD | |
| ISOMOS2 | ISOMOS | |
| HVDEPL | NHVE | |
| HIGHTEMP | | PHOTODIO |
| PHOTODIO | ISOMOS | HIGHTEMP |
| NVM | ISOMOS | FLATPV, SFLATPV |
| ANODOP | UVWINDOW | MET4, METTHK |
| CATDOP | UVWINDOW | MET4, METTHK |
| UVWINDOW * | MET3+METMID | MET4, METTHK |

* Only allowed with (ANODOP or CATDOP)

XH018 RESTRICTION FOR MODULE COMBINATIONS (CONT')

| Module name | Use of the module also requires use of the following module(s) | Use of the module is not available with the use of the following module(s) |
|-------------|--|--|
| FLASH | NVM | FLATPV, SFLATPV |
| DMOS | HVMOS | |
| NHVE | HVNMOS | |
| PHVE | HVPMOS | |
| OTP3 | | FLATPV, SFLATPV |
| MIM23 | MET3 | MIM34, MIMH23, MIMH34, MIM, DMIM, TMIM, MIMH, DMIMH, TMIMH |
| MIM34 | MET4 | MIM23, MIMH23, MIMH34, MIM, DMIM, TMIM, MIMH, DMIMH, TMIMH |
| MIMH23 | MET3 | MIM23, MIM34, MIMH34, MIM, DMIM, TMIM, MIMH, DMIMH, TMIMH |
| MIMH34 | MET4 | MIM23, MIM34, MIMH23, MIM, DMIM, TMIM, MIMH, DMIMH, TMIMH |
| MIM | METMID | MIM23, MIM34, MIMH23, MIMH34, DMIM, TMIM, MIMH, DMIMH, TMIMH |
| DMIM | MET3 | MIM23, MIM34, MIMH23, MIMH34, MIM, TMIM, MIMH, DMIMH, TMIMH |
| TMIM | MET4 | MIM23, MIM34, MIMH23, MIMH34, MIM, DMIM, MIMH, DMIMH, TMIMH |
| MIMH | METMID | MIM23, MIM34, MIMH23, MIMH34, MIM, DMIM, TMIM, DMIMH, TMIMH |
| DMIMH | MET3 | MIM23, MIM34, MIMH23, MIMH34, MIM, DMIM, TMIM, MIMH, TMIMH |
| TMIMH | MET4 | MIM23, MIM34, MIMH23, MIMH34, MIM, DMIM, TMIM, MIMH, DMIMH |
| MET4 | MET3 | |
| MET5 | MET4 | METTHK |
| METTHK | METMID | MET5 |
| FLATPV | METMID | METTHK, NVM, FLASH, OTP3, SFLATPV |
| SFLATPV | METMID | METTHK, NVM, FLASH, OTP3, FLATPV |

XH018 METAL OPTIONS

| Number of Metals | Available Metal Layer Combinations | Module Names |
|------------------|--|-------------------------------|
| 4 | MET1 - MET2 - MET3 - METTP | LPMOS+MET3+METMID |
| 5 | MET1 - MET2 - MET3 - MET4 - METTP | LPMOS+MET3+MET4+METMID |
| 5 | MET1 - MET2 - MET3 - METTP - METTPL | LPMOS+MET3+METMID+METTHK |
| 6 | MET1 - MET2 - MET3 - MET4 - MET5 - METTP | LPMOS+MET3+MET4+MET5+METMID |
| 6 | MET1 - MET2 - MET3 - MET4 - METTP - METTPL | LPMOS+MET3+MET4+METMID+METTHK |

Active Devices

| XH018 LOW NOISE TRANSISTORS | | | | | | | |
|------------------------------|--|--|---------|-----------------------------------|----------------------------------|----------|--------------|
| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | IOFF [$\text{pA}/\mu\text{m}$] | BVDS [V] | Max. VDS [V] |
| 1.8V low noise NMOS | nelna | ULN | 0.61 | 460 | < 3 | > 3.6 | 1.98 |
| | nelnai ⁽¹⁾ | ULN+ISOMOS | 0.6 | | | | |
| | nelnai_6 ⁽²⁾ | ULN+(ISOMOS2, ISOMOS+HVMOS) | 0.6 | | | | |
| | nelnai_m_6 ⁽²⁾ | ULN+ISOMOS | 0.6 | | | | |
| 3.3V low noise NMOS | ne3lna | ULN | 0.74 | 580 | < 3 | > 5 | 3.6 |
| | ne3lnai ⁽¹⁾ | ULN+ISOMOS | 0.72 | 590 | | | |
| | ne3lnai_6 ⁽²⁾ | ULN+(ISOMOS2, ISOMOS+HVMOS) | 0.72 | 590 | | | |
| | ne3lnai_m_6 ⁽²⁾ | ULN+ISOMOS | 0.72 | 590 | | | |
| 3.3V low noise PMOS | pe3lna, pe3lna_5 ⁽²⁾ | ULN | 0.63 | 300 | < 3 | > 5 | 3.6 |
| 3.3V isolated low noise PMOS | pe3lnai ⁽¹⁾ , pe3lnai_5 ⁽²⁾ , pe3lnai_m_5 ⁽²⁾ | ULN+ISOMOS ULN+(ISOMOS2, ISOMOS+HVMOS) ULN+ISOMOS | 0.63 | 300 | < 3 | > 5 | 3.6 |
| 3.3V low noise PMOS | pe3ln, pe3ln_5 ⁽²⁾ | LNP MOS3 | 0.92 | 250 | < 15 | > 5 | 3.6 |
| 3.3V isolated low noise PMOS | pe3lni ⁽¹⁾ , pe3lni_5 ⁽²⁾ , pe3lni_m_5 ⁽²⁾ | LNP MOS3+ISOMOS LNP MOS3+(ISOMOS2, ISOMOS+HVMOS) LNP MOS3+ISOMOS | 0.92 | 250 | < 15 | > 5 | 1.98 |

⁽¹⁾ The ISOMOS2 or HVMOS module is needed, if isolated MOS transistors are placed in DNWELL instead of DNWELLMV.
⁽²⁾ These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

| XH018 MOS CORE TRANSISTORS | | | | | | | | |
|----------------------------|---------------------------|-----------------------|---------|-----------------------------------|----------------------------------|----------|--------------|--------------|
| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | IOFF [$\text{pA}/\mu\text{m}$] | BVDS [V] | Max. VDS [V] | Max. VGS [V] |
| 1.8V LP NMOS | ne | LPMOS | 0.58 | 475 | < 3 | > 3.6 | 1.98 | 1.98 |
| 1.8V LP PMOS | pe, pe_5 ⁽²⁾ | LPMOS | 0.65 | 170 | < 3 | > 3.6 | 1.98 | 1.98 |
| 3.3V native Vt NMOS | nn3 | LPMOS | 0.18 | 650 | - | > 4 | 3.6 | 3.6 |
| 3.3V LP NMOS | ne3 | LPMOS | 0.69 | 605 | < 3 | > 5 | 3.6 | 3.6 |
| 3.3V LP PMOS | pe3, pe3_5 ⁽²⁾ | LPMOS | 0.63 | 305 | < 3 | > 5 | 3.6 | 3.6 |

⁽²⁾ These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

| XH018 MEDIUM & LOW VT TRANSISTORS | | | | | | | | |
|-----------------------------------|-------------------------------|-----------------------|---------|-----------------------------------|----------------------------------|----------|--------------|--------------|
| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | IOFF [$\text{pA}/\mu\text{m}$] | BVDS [V] | Max. VDS [V] | Max. VGS [V] |
| 1.8V SVT NMOS | nesvt, | SVT | 0.47 | 550 | < 40 | > 3.6 | 1.98 | 1.98 |
| 1.8V SVT PMOS | pesvt, pesvt_5 ⁽²⁾ | SVT | 0.48 | 255 | < 40 | > 3.6 | 1.98 | 1.98 |
| 1.8V LVT NMOS | nel | LVT | 0.35 | 610 | < 5k | > 3.6 | 1.98 | 1.98 |
| 1.8V LVT PMOS | pel, pel_5 ⁽²⁾ | LVT | 0.36 | 300 | < 10k | > 3.6 | 1.98 | 1.98 |

⁽²⁾ These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

Active Devices (Continued)

| XH018 ISOMOS TRANSISTORS | | | | | | | |
|--------------------------|---|---|---------|-----------------------------------|----------------------------------|-----------|--------------|
| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | IOFF [$\text{pA}/\mu\text{m}$] | BVDS [V] | max. VDS [V] |
| Iso. 1.8V SVT PMOS | nesvti ⁽¹⁾ , nesvti_6 ⁽²⁾ , nesvti_m_6 ⁽²⁾ | SVT+ISOMOS SVT+(ISOMOS2, ISOMOS+HVMOS) SVT+ISOMOS | 0.46 | 550 | < 40 | > 3.6 | 1.98 |
| Iso. 1.8V SVT PMOS | pesvti ⁽¹⁾ , pesvti_6 ⁽²⁾ , pesvti_m_6 ⁽²⁾ | SVT+ISOMOS SVT+(ISOMOS2, ISOMOS+HVMOS) SVT+ISOMOS | 0.48 | 255 | < 40 | > 3.6 | 1.98 |
| Iso. 1.8V LP NMOS | nei ⁽¹⁾ , nei_m_6 ⁽²⁾ , nei_6 ⁽²⁾ | ISOMOS ISOMOS2, ISOMOS+HVMOS | 0.58 | 475 | < 3 | > 3.6 | 1.98 |
| Iso. 1.8V LP PMOS | pei ⁽¹⁾ , pei_m_5 ⁽²⁾ , pei_5 ⁽²⁾ | ISOMOS ISOMOS2, ISOMOS+HVMOS | 0.65 | 170 | < 3 | > 3.6 | 1.98 |
| Iso. 1.8V LVT NMOS | neli ⁽¹⁾ , neli_m_6 ⁽²⁾ , neli_6 ⁽²⁾ | LVT+ISOMOS LVT+(ISOMOS2, ISOMOS+HVMOS) | 0.35 | 610 | < 5k | > 3.6 | 1.98 |
| Iso. 1.8V LVT PMOS | pe1i ⁽¹⁾ , pe1i_m_5 ⁽²⁾ , pe1i_5 ⁽²⁾ | LVT+ISOMOS LVT+(ISOMOS2, ISOMOS+HVMOS) | 0.36 | 300 | < 10k | > 3.6 | 1.98 |
| Iso. 3.3V LP NMOS | ne3i ⁽¹⁾ , ne3i_m_6 ⁽²⁾ , ne3i_6 ⁽²⁾ | ISOMOS ISOMOS2, ISOMOS+HVMOS | 0.665 | 615 | < 3 | > 5.0 | 3.6 |
| Iso. 3.3V LP PMOS | pe3i ⁽¹⁾ , pe3i_m_5 ⁽²⁾ , pe3i_5 ⁽²⁾ | ISOMOS ISOMOS2, ISOMOS+HVMOS | 0.63 | 305 | < 3 | > 5.0 | 3.6 |

⁽¹⁾ The ISOMOS2 or HVMOS module is needed, if isolated MOS transistors are placed in DNWELL instead of DNWELLMV.
⁽²⁾ These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

| XH018 MEDIUM VOLTAGE TRANSISTORS | | | | | | | | | |
|----------------------------------|-------------------|-----------------------|---------|-----------------------------------|--|--|-----------|----------------|--------------|
| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | RON [$\text{k}\Omega\cdot\mu\text{m}$] | RON*A [$\text{m}\Omega\cdot\text{mm}^2$] | BVDSS [V] | Max. VDS [V] | Max. VGS [V] |
| 6V NMOS | nma nma_bjt* | HVNMOS | 1.23 | 140 | 3.6 | | > 8.5 | 6 | 18 |
| 6V PMOS | pma pma_bjt* | HVPMOS | 1.20 | 55 | 13 | | > 8.5 | 6 | 18 |
| 10V HV NMOS | nmma nmma_bjt* | HVMOS | 1.45 | 52 | 13 | 60.5 | > 15 | 10 | 10 |
| 10V Asy. HV NMOS | nmc nmc_bjt* | NHVE | 1.40 | 80 | 13 | | > 21 | 10 | 18 |
| 15V HV PMOS | pmma pmma_bjt* | HVMOS | 1.50 | 19.5 | 43 | 202 | > 20 | 15 | 15 |
| 15V Sym. HV NMOS | nmmc nmmc_bjt* | NHVE | 1.32 | 41 | 22 | 99 | > 21 | 15 | 18 |
| 15V Sym. HV NMOS | nmmd nmmd_bjt* | NHVE | 1.70 | 46 | 20 | 112 | > 21 | 15 | 18 |
| 20V Sym. HV PMOS | pmmc pmmc_bjt* | PHVE | 1.40 | 21 | 54 | 228 | > 24 | 20 | 18 |
| 20V Asy. HV PMOS | pmc pmc_bjt* | PHVE | 1.15 | 47 | 34 | | > 24 | 20 | 18 |
| 5V ESD PMOS | pmb** | HVMOS | - | - | - | - | - | - | - |

* These devices are variants of the corresponding basic devices with parasitic substrate PNP and underlying wells. Parameters of these devices are identical to the corresponding basic devices.
** This device is only allowed to be used for ESD protection. Please refer to ESD documentation on "My X-FAB".

Active Devices (Continued)

XH018 DEPLETION TRANSISTORS

| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | BVDSS [V] | Max. VDS [V] | Max. VGS [V] |
|---------------------|---|--|---------|-----------------------------------|-----------|----------------|--------------|
| 3.3V Depl NMOS | nd3 | DEPL | 0.20 | 730 | > 5 | 3.6 | 3.6 |
| Iso. 3.3V Depl NMOS | nd3i ⁽¹⁾ nd3i_6 ⁽²⁾ nd3i_m_6 ⁽²⁾ | DEPL+ (ISOMOS, HVMOS) DEPL+HVMOS DEPL+ISOMOS | 0.24 | 740 | > 5 | 3.6 | 3.6 |

⁽¹⁾ The ISOMOS2 or HVMOS module is needed, if isolated MOS transistors are placed in DNWELL instead of DNWELLMV.

⁽²⁾ These devices are variants of the corresponding basic device with underlying wells. Parameters of these devices are identical to the corresponding basic device.

XH018 HIGH VOLTAGE DEPLETION TRANSISTORS

| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | RON [$\text{k}\Omega\cdot\mu\text{m}$] | RON*A [$\text{m}\Omega\cdot\text{mm}^2$] | BVDSS [V] | Max. VDS [V] | Max. VGS [V] |
|-----------------------|---------------------|-----------------------|---------|-----------------------------------|--|--|-----------|----------------|--------------|
| 32V Asy. HV Depl NMOS | nhvd nhvd_bjt* | HVDEPL | 1.15 | 7.5 | 37 | 167 | > 50 | 32 | 18 |
| 32V Sym. HV Depl NMOS | nhhvd nhhvd_bjt* | HVDEPL | 1 | 3 | 53 | 514 | > 50 | 32 | 18 |

* These devices are variants of the corresponding basic devices with parasitic substrate PNP and underlying wells. Parameters of these devices are identical to the corresponding basic devices.

XH018 HIGH VOLTAGE TRANSISTORS

| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | RON [$\text{k}\Omega\cdot\mu\text{m}$] | RON*A [$\text{m}\Omega\cdot\text{mm}^2$] | BVDSS [V] | Max. VDS [V] | Max. VGS [V] |
|------------------|-------------------|-----------------------|---------|-----------------------------------|--|--|-----------|----------------|--------------|
| 45V Sym. HV NMOS | nhhv nhhv_bjt* | NHVE | 1.87 | 62 | 60 | 686 | > 50.5 | 45 | 18 |
| 45V Sym. HV PMOS | phhv phhv_bjt* | PHVE | 1.5 | 39 | 101 | 900 | > 51 | 45 | 18 |
| 45V Asy. HV NMOS | nhv nhv_bjt* | NHVE | 1.63 | 130 | 33 | 214 | > 50.5 | 45 | 18 |
| 45V Asy. HV PMOS | phv phv_bjt* | PHVE | 1.38 | 102 | 56 | 280 | > 51 | 45 | 18 |

* These devices are variants of the corresponding basic devices with parasitic substrate PNP and underlying wells. Parameters of these devices are identical to the corresponding basic devices.

XH018 DMOS TRANSISTORS

| Device | Name | Available with module | VT [V] | IDS [$\mu\text{A}/\mu\text{m}$] | RON [$\text{k}\Omega\cdot\mu\text{m}$] | RON*A [$\text{m}\Omega\cdot\text{mm}^2$] | BVDSS [V] | Max. VDS [V] | Max. VGS [V] |
|------------------|-----------------------|-----------------------|---------|-----------------------------------|--|--|-----------|----------------|--------------|
| Iso. 40V nLDMOS* | nedi** nedi_bjt* | DMOS | 1.63 | 110 | 15 | 60 | > 45.5 | 40 | 18 |
| 35V pLDMOS | ped2 ped2_bjt* | DMOS | 2.0 | 42 | 42 | 185 | > 40.5 | 35 | 18 |
| Iso. 45V nLDMOS | nedia** nedia_bjt* | DMOS | 1.65 | 82 | 19 | 114 | > 55 | 45 | 18 |
| 45V pLDMOS | ped ped_bjt* | DMOS | 1.95 | 41 | 48 | 215 | > 50.5 | 45 | 18 |

** 'nedi' has been superseded by 'nedia'. 'nedia' is a more robust device with higher on-state drain-source breakdown voltage than 'nedi'

* Parameters of these devices are identical to the corresponding basic devices.

Active Devices (Continued)

| XH018 BIPOLAR TRANSISTORS | | | | | | | | |
|---------------------------|-----------|-----------------------|------|--------|-----------|----------|--------------|----------|
| Device | Name | Available | BETA | VA [V] | BVCEO [V] | VBE [mV] | max. VCE [V] | VEB [V] |
| 1.8V vPNP | qpva | LPMOS | 2.5 | 250 | | 710 | 1.98 | 1.5 |
| | qpvb | | 2.6 | 150 | | 669 | | |
| | qpvc | | 2.8 | 100 | | 636 | | |
| 3.3V vPNP | qpva3 | LPMOS | 2.3 | 250 | | 709 | 3.6 | 1.5 |
| | qpvb3 | | 2.5 | 150 | | 669 | | |
| | qpvc3 | | 2.7 | 100 | | 635 | | |
| ESD HV PNP | qpvhscr* | BIPESD | 31 | | > 51 | 574 | 45 | 45 |
| ESD HV PNP | qpvascr* | HVMOS+DMOS | - | - | - | - | - | - |
| ESD HV PNP | qpvhbscr* | ESDPNP | 13.5 | | > 51 | 570 | 45 | 25 |
| 3.3V vNPN | qnva | DEPL+HVMOS | > 21 | 16 | > 10 | 710 | 3.6 | 2.5 |
| 3.3V vNPN | qnvb | DEPL+ (ISOMOS, HVMOS) | 85 | 8.5 | > 4.5 | 700 | 3.6 | 2.5 |
| 3.3V vNPN | qnvc | ISOMOS | 18.5 | 79 | > 10 | 695 | 3.6 | 2.5 |

* These devices are only allowed to be used for ESD protection. Please refer to ESD documentation on "My X-FAB".

Passive Devices

| XH018 POLY RESISTORS | | | | | |
|-----------------------|-----------------|-----------------------|-------------------------|------------------------------|-------------|
| Device | Name | Available with module | RS [Ω/\square] | Temp. Coeff. [$10^{-3}/K$] | Max VTB [V] |
| N+ Poly | rnp1, rnp1_3* | LPMOS | 320 | -1.38 | 45 |
| P+ Poly | rpp1, rpp1_3* | LPMOS | 280 | -0.11 | 45 |
| P+ Poly silicided | rpp1s, rpp1s_3* | LPMOS | 7.5 | 2.92 | 45 |
| High-Ohmic N+ Poly1 | rnp1h, rnp1h_3* | LPMOS | 6300 | -4 | 45 |
| Lightly dope P+ Poly1 | rpp1k, rpp1k_3* | MRPOLY | 960 | -0.85 | 45 |

* These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realize an improved description of bulk voltage dependency.

| XH018 DIFFUSION RESISTORS | | | | | |
|---------------------------|-----------------|-----------------------|-------------------------|------------------------------|-------------|
| Device | Name | Available with module | RS [Ω/\square] | Temp. Coeff. [$10^{-3}/K$] | Max VTB [V] |
| 1.8V N+ diffusion | rdn | LPMOS | 65 | 1.42 | 1.98 |
| | rdn_esd* | HVMOS | | | |
| 1.8V P+ diffusion | rdp | LPMOS | 130 | 1.3 | 1.98 |
| | rdp_io* | HVMOS | | | |
| 1.8V N-well | rnw, rnw_scr* | LPMOS | 970 | 2.90 | 5.5 |
| 3.3V N+ diffusion | rdn3 | LPMOS | 61 | 1.42 | 3.6 |
| 3.3V P+ diffusion | rdp3 | LPMOS | 125 | 1.3 | 3.6 |
| 3.3V N-well | rnw3, rnw3_scr* | LPMOS | 970 | 2.90 | 5.5 |
| 5V Deep N-well | rdnwmv | ISOMOS, HVMOS | 1500 | 5.6 | 5.5 |

* These devices are only allowed to be used for ESD protection. Please refer to ESD documentation on "My X-FAB".

Passive Devices (Continued)

| XH018 METAL RESISTORS | | | | | | | |
|-----------------------|-------|-----------------------|-------------------------|-----------------------------|------------------------------|-------------------------------------|-------------|
| Device | Name | Available with module | RS [Ω/\square] | Thickness [μm] | Max J/W [mA/ μm] | Temp. Coeff. [$10^{-3}/\text{K}$] | Max VTB [V] |
| Metal 1 | rm1 | LPMOS | 0.077 | 0.555 | 0.5* | 3.4 | 45 |
| Metal 2 | rm2 | LPMOS | 0.074 | 0.565 | 0.5* | 3.4 | 45 |
| Metal 3 | rm3 | MET3 | 0.074 | 0.565 | 0.5* | 3.4 | 45 |
| Metal 4 | rm4 | MET4 | 0.074 | 0.565 | 0.5* | 3.4 | 45 |
| Metal 5 | rm5 | MET5 | 0.074 | 0.565 | 0.5* | 3.4 | 45 |
| Top Metal | rmtp | METMID | 0.031 | 0.98 | 1.6* | 3.2 | 45 |
| Thick Metal | rmtpl | METTHK | 0.0101 | 3.11 | 6** | 3.8 | 45 |

* value quoted at Tj = -40°C ... +175°C; value for Tj = -40°C ... +125°C is 1.0 mA/ μm
 ** value quoted for both Tj = -40°C ... +175°C and Tj = -40°C ... +125°C

| XH018 VARACTORS | | | | | | |
|----------------------|-----------|--------------------------|------------------|--|--|----------------|
| Device | Name | Available with module | Tuning range [%] | Capacitance @-V [fF/ μm^2] | Capacitance @+V [fF/ μm^2] | Max VBpsub [V] |
| 1.8V N-type varactor | mosvc | LPMOS | 70 | 2.6 | 8.1 | 5.5 |
| 3.3V N-type varactor | mosvc3 | LPMOS | 70 | 1.7 | 5 | 5.5 |
| 3.3V P-type varactor | mosvc3i | ISOMOS2, ISOMOS+HVMOS | 70 | 5 | 1.6 | 45 |
| 3.3V P-type varactor | mosvc3i_m | ISOMOS | 70 | 5 | 1.6 | 10 |
| 1.8V P-type varactor | mosvci | ISOMOS2, ISOMOS+HVMOS | 75 | 8.1 | 2 | 45 |
| 1.8V P-type varactor | mosvci_m | ISOMOS | 75 | 8.1 | 2 | 10 |

| XH018 SANDWICH CAPACITORS | | | | |
|---------------------------|----------|-----------------------|---------------------------------|--------------|
| Device | Name | Available with module | Area Cap [fF/ μm^2] | Max. VTB [V] |
| Poly1/M1/M2/M3 | csandwt3 | MET3 | 0.155 | 45 |
| Poly1/M1/M2/M3/M4 | csandwt4 | MET4 | 0.2 | 45 |
| Poly1/M1/M2/M3/M4/M5 | csandwt5 | MET5 | 0.25 | 45 |

| XH018 POD CAPACITOR | | | | | | |
|---------------------|--------|--|----------------------------------|----------------|---------|--------------|
| Device | Name | Available with module | Area Cap. [fF/ μm^2] | V Coeff. [1/V] | BV [V] | max. VTB [V] |
| 1.8V POD capacitor | cpod | CPOD | 7.7 | 90k | > 3 | 1.98 |
| 3.3V POD capacitor | cpod3 | CPOD | 4.3 | 26k | > 5 | 3.6 |
| HV POD capacitor | cpodhv | CPODHV, CPOD+(HVMOS, HVN- MOS, HVPMOS, ESDPNP) | 1 | 1.7k | > 30 | 18 |

Passive Devices (Continued)

| XH018 FRINGE CAPACITORS | | | | | | |
|-------------------------------|--------|-----------------------|---------------|--------|--------------|--|
| Device | Name | Available with module | Cell Cap [fF] | BV [V] | Max. VTB [V] | |
| Poly1/M1/M2 fringe | csf2p | LPMOS | 25.2 | > 15 | 45 | |
| Poly1/M1/M2/M3 fringe | csf3p | MET3 | 36.8 | > 15 | 45 | |
| 10V M1/M2/M3 fringe | csf3 | MET3 | 32.9 | > 35 | 45 | |
| 45V M1/M2/M3 fringe | csf3a | MET3 | 23.9 | > 70 | 45 | |
| 10V M1/M2/M3/M4 fringe | csf4 | MET4 | 45 | > 35 | 45 | |
| 45V M1/M2/M3/M4 fringe | csf4a | MET4 | 32.9 | > 70 | 45 | |
| 10V M1/M2/M3/M4/M5 fringe | csf5 | MET5 | 57.1 | > 35 | 45 | |
| 45V M1/M2/M3/M4/M5 fringe | csf5a | MET5 | 41.8 | > 70 | 45 | |
| 10V M1/M2/M3/MTP fringe | csft4 | MET3+METMID | 36.5 | > 35 | 45 | |
| 45V M1/M2/M3/MTP fringe | csft4a | MET3+METMID | 28.7 | > 70 | 45 | |
| 10V M1/M2/M3/M4/MTP fringe | csft5 | MET4+METMID | 49.1 | > 35 | 45 | |
| 45V M1/M2/M3/M4/MTP fringe | csft5a | MET4+METMID | 37.7 | > 70 | 45 | |
| 10V M1/M2/M3/M4/M5/MTP fringe | csft6 | MET5+METMID | 61.5 | > 35 | 45 | |
| 45V M1/M2/M3/M4/M5/MTP fringe | csft6a | MET5+METMID | 46.6 | > 70 | 45 | |

| XH018 MIM CAPACITOR | | | | | | |
|---|----------------------------|--|--------------------------------|----------------|---------|--------------|
| Device | Name | Available with module | Area Cap [fF/μm ²] | V Coeff. [1/V] | BV [V] | max. VTB [V] |
| Single MIM, M2/M3 | cmm3 | MIM23 | 1.00 | -15 | > 20 | 45 |
| Single MIM, M3/M4 | cmm4 | MIM34 | 1.00 | -15 | > 20 | 45 |
| Single MIM, M3/MTP Single MIM, M4/MTP Single MIM, M5/MTP | cmm4t cmm5t cmm6t | MET3+METMID+MIM MET4+METMID+MIM MET5+METMID+MIM | 1.00 | -15 | > 20 | 45 |
| Double MIM, M2/M3/MTP Double MIM, M2/M3/M4 | cdmm4t cdmm4 | MET3+METMID+DMIM MET4+DMIM | 2.00 | 3 | > 20 | 45 |
| Triple MIM, M2/M3/M4/MTP Triple MIM, M2/M3/M4/M5 | ctmm5t ctmm5 | MET4+ METMID+ TMIM MET5+TMIM | 3.00 | 15 | > 20 | 45 |
| High cap. MIM, M2/M3 | cmmh3 | MIMH23 | 2.35 | -120 | > 10 | 45 |
| High cap. MIM, M3/M4 | cmmh4 | MIMH34 | 2.35 | -120 | > 10 | 45 |
| High cap. MIM, M3/MTP High cap. MIM, M4/MTP High cap. MIM, M5/MTP | cmmh4t cmmh5t cmmh6t | MET3+METMID+MIMH MET4+METMID+MIMH MET5+METMID+MIMH | 2.35 | -120 | > 10 | 45 |
| High cap. DMIM, M2/M3/MTP High cap. DMIM, M2/M3/M4 | cdmmh4t cdmmh4 | MET3+METMID+DMIMH MET4+DMIMH | 4.70 | -20 | > 10 | 45 |
| High cap. TMIM M2/M3/M4/MTP High cap. TMIM M2/M3/M4/M5 | ctmmh5t ctmmh5 | MET4+METMID+TMIMH MET5+TMIMH | 7.05 | -120 | > 10 | 45 |

| XH018 SCHOTTKY DIODE | | | | | | |
|----------------------|------|-----------------------|--------------|---------------|---------|--------------|
| Device | Name | Available with module | Vforward [V] | ILeakage [nA] | BV [V] | Max. VTB [V] |
| 18V Schottky | dsb | SCHOTTKY | 0.45 | < 5 | > 20.5 | 45 |

Passive Devices (Continued)

| XH018 PROTECTION DIODES | | | | | | |
|-------------------------|-------|-----------------------|----------------------|--------|-----------------------|-------------|
| Device | Name | Available with module | Leakage Current [pA] | BV [V] | BV Temp. Coef. [mV/K] | Max Vcc [V] |
| 20V N-type Protection | dnp20 | NHVE | 300 | > 23 | 10 | 30 |
| 20V P-type Protection | dpp20 | HVMOS | 100 | > 22 | 18 | 30 |

| XH018 PHOTO DIODES | | | | | |
|---|-------|-----------------------|---|-----------------------------|-------------|
| Device | Name | Available with module | Area dark Current [aA/μm ²] | Sensitivity [A/W] | Max Vcc [V] |
| PD for visible & infrared light detection | dphoa | PHOTODIO | 0.1 | 0.35 / 0.42 / 0.31* | 10 |
| PD for infrared light detection | dphob | PHOTODIO | 1.9 | 0.03 / 0.24 / 0.25* | 10 |
| PD for UV light detection | dphoc | CATDOP+ UVWINDOW | 0.7 | 0.11 / 0.23 / 0.39 / 0.26** | 10 |
| PD for UV light detection | dphod | ANODOP+ UVWINDOW | 0.2 | 0.11 / 0.21 / 0.07 / 0.01** | 5 |

* optical responsibility @500nm / @650nm / @850nm
 ** optical responsibility @300nm / @405nm / @650nm / @850nm

| XH018 DIFFUSION DIODE | | | | | | |
|-----------------------|----------|-----------------------|--------------------------------|--------|---------------------------------------|-------------|
| Device | Name | Available with module | Area Cap [fF/μm ²] | BV [V] | Leakage Current [fA/μm ²] | Max VCC [V] |
| Polysilicon | dpol | LPMOS | - | - | - | - |
| 1.8V N+ diff. /PW1 | dn | LPMOS | 1.11 | > 6 | 0.042 | 1.98 |
| 1.8V P+ diff. /NW1 | dp | LPMOS | 1.02 | > 6 | 0.002 | 1.98 |
| 1.8V NW1 /Psub | dnw | LPMOS | 0.1 | > 9 | 0.0001 | 5.5 |
| 3.3V N+ diff. /PW2 | dn3 | LPMOS | 0.87 | > 6 | 0.006 | 3.6 |
| 3.3V P+ diff. /NW2 | dp3 | LPMOS | 1.00 | > 6 | 0.0007 | 3.6 |
| 3.3V NW2 /Psub | dnw3 | LPMOS | 0.1 | > 9 | 0.0001 | 5.5 |
| MV DNW /P+ diff. | ddnwmv | ISOMOS, HVMOS | 0.07 | > 15 | 0.0001 | 10 |
| P+ diff. /MV DNW | dpdnwmv | ISOMOS, HVMOS | 0.56 | > 10 | 0.01 | 5.5 |
| Iso. PW /MV DNW | dipdnwmv | ISOMOS, HVMOS | 0.34 | > 15 | 0.003 | 8 |
| DNW /Psub | ddnw | HVMOS | 0.06 | > 80 | 0.0002 | 45 |
| Iso. P+ diff. /DNW | dpdnw | HVMOS | 0.56 | > 10 | 0.003 | 5.5 |
| Iso. PW /DNW | dipdnw | HVMOS, ISOMOS | 0.36 | > 15 | 0.0003 | 8 |
| N+ diff. /HV PW | dnhpw | HVMOS | 0.77 | > 9 | 0.01 | 5.5 |
| P+ diff. /HV NW | dphnw | HVMOS | 0.62 | > 9 | 0.01 | 5.5 |
| HV PW /DNW | dhpw | HVMOS | 0.25 | > 20 | 0.002 | 15 |
| HV NW /Psub | dhnw | HVMOS | 0.1 | > 47 | 0.0001 | 15 |
| NDF /Psub | dndf | NHVE | 0.08 | > 50.5 | 0.0001 | 45 |
| PDF /HV NW | dpdwhn | PHVE | 0.21 | > 50 | 0.006 | 45 |
| HV NW /Psub | dwhn | HVPMOS | 0.07 | > 50 | 0.0001 | 45 |
| P+ diff. /HV NW | dpwhn | HVPMOS | 0.21 | > 22 | 0.0014 | 20 |
| N+ diff. /Psub | dnn3 | LPMOS | 0.07 | | 0.033 | |

Non-Volatile-Memory

| XH018 POLY FUSE | | | | | | |
|-----------------|-------|-----------------------|------------------|-----------------|-------------------|---------------------|
| Device | Name | Available with module | Unprog. Res. [Ω] | Prog. Res. [kΩ] | Prog. Max VCC [V] | Unprog. Max VCC [V] |
| Poly fuse | pfuse | LPMOS | 35 | > 100 | 3.6 | 0.1 |

| XH018 NVM | | | |
|-----------------------|--|--|-----------------------|
| Parameter | NVRAM Compiler | Flash | TrimOTP Compiler |
| Available with module | NVM+MIM | NVM+FLASH+MIM | OTP3 |
| Memory Size | 1k to 16k bits | 8k x32 | 8 to 16k bits |
| Operating voltage | 1.6 to 2.0V 3.0 to 3.6V | 1.6 to 2.0V 3.0 to 3.6V | 3.0 to 3.6V |
| Operating temperature | -40 to +175°C | -40 to +175°C read -40 to +125°C NV write/erase | -40 to +175°C |
| Endurance | 100k cycles for EEPROM @25°C 10k cycles for EEPROM @150°C unlimited SRAM | 1k cycles @125°C | |
| Data retention | Min. 10 years @ 125°C Min 3 year @150°C Min 1 years @175°C | Min. 10 years @125°C Min. 3 years @150°C Min. 1 years @175°C | Min. 20 years @ 125°C |

I/O LIBRARIES

| XH018 I/O CELLS LIBRARY | | | | | | |
|-------------------------|--|---------------------|-------------------|-----------|----------------------|--|
| Device | Library Feature | V _{CORE} * | V _{IO} * | ESD Level | Application benefits | |
| IO_CELLS_3V | Standard, 3.3V/1.8V multi supply voltage | 1.8V | 3.3V | 4kV HBM | Pad limited | |
| IO_CELLS_F3V | Standard, 3.3V/1.8V multi supply voltage | 1.8V | 3.3V | 2kV HBM | Core limited | |
| IO_CELLS_C1V8 | Standard, V _{CORE} =V _{IO} single supply voltage | 1.8V | 1.8V | 4kV HBM | Pad limited | |
| IO_CELLS_FC1V8 | Standard, V _{CORE} =V _{IO} single supply voltage | 1.8V | 1.8V | 2kV HBM | Core limited | |
| IO_CELLS_C3V | Standard, V _{CORE} =V _{IO} single supply voltage | 3.3V | 3.3V | 4kV HBM | Pad limited | |
| IO_CELLS_FC3V | Standard, V _{CORE} =V _{IO} single supply voltage | 3.3V | 3.3V | 2kV HBM | Core limited | |
| IO_CELLS_JI3V | Junction isolated, 1.8V/3.3V multi supply voltage | 1.8V | 3.3V | 4kV HBM | Pad limited | |

* Please refer to the library databook for details about available PVT ranges

| XH018 HV CELLS LIBRARY | | | | |
|------------------------|--|---------------|-------------|-----------------------|
| Device | Library Feature | Voltage Range | ESD Level | Application benefits |
| HV_CELLS | Special LV I/O, operating voltage specific HV ESD protection cells | LV, 12V-58V | 2kV-8kV HBM | Customized I/O Design |

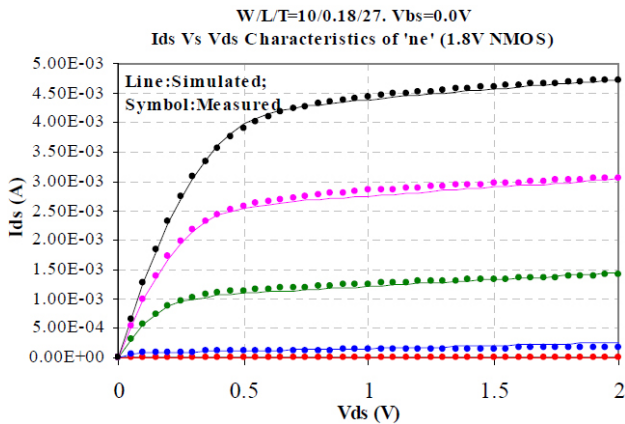
STANDARD CELLS LIBRARIES

| XH018 STD CELLS LIBRARY | | | |
|-------------------------|---|---------------------|--|
| Device | Library feature | Voltage range | Application benefits |
| D_CELLS | Standard Speed & Low Power | 1.8V | standard speed, low power cells available, P&R compatible with D_CELLS_LL, D_CELLS_MV |
| D_CELLS_LL | Low Leakage & Low Power | 1.8V | low leakage (0.21um channel length), low power cells (X0) available, P&R compatible with D_CELLS |
| D_CELLS_HD | Standard Speed & Low Power, High Density routing pitch | 1.8V / 1.2V | standard speed, high density routing pitch, low power cells available, P&R compatible with D_CELLS_HDMV |
| D_CELL_3V | Standard Speed & Low Power, High Density routing pitch | 3.3V / 2.2V | 3.3V, 2.2V supply, standard speed, low power cells available, high density routing pitch |
| D_CELLS_JI | Junction Isolated, Standard Speed & Low Power | 1.8V | standard speed, low power cells (X0) available, noise protection |
| D_CELLS_JILL | Junction Isolated, Low Leakage & Low Power | 1.8V / 1.2V | low leakage (0.21um channel length), low power cells available, noise protection, voltage shifting, P&R compatible with D_CELLS_JI, D_CELLS_JIMV |
| D_CELLS_JIHD | Junction Isolated, Standard Speed & Low Power, High Density routing pitch | 1.8V / 1.2V | standard speed, high density routing pitch, low power cells available, noise protection, voltage shifting, P&R compatible with D_CELLS_JIHDMV |
| D_CELLS_JI3V | Junction Isolated, Standard Speed & Low Power, High Density routing pitch | 3.3V / 2.2V | 3.3V, 2.2V supply, standard speed, low power cells (X0) available, high density routing pitch, noise protection |
| D_CELLSL_JI3V | Junction Isolated, Low Power | 3.3V / 2.2V | low power consumption, noise protection, voltage shifting, P&R compatible with D_CELLSL_JIM3V |
| D_CELLS_MV | Multi Supply Voltage, Power Shut Off | 1.8V/ 1.2V ... 3.3V | standard speed & power, multivoltage |
| D_CELLS_HDMV | Multi Supply Voltage, Power Shut Off, High Density routing pitch | 1.8V/ 1.2V ... 3.3V | standard speed & power, multivoltage, high density routing pitch |
| D_CELLS_JIHDMV | Junction Isolated, Multi Supply Voltage, Power Shut Off, High Density routing pitch | 1.8V/ 1.2V ... 3.3V | standard speed & power, multivoltage, noise protection, voltage shifting, |
| D_CELLS_JIMV | Junction Isolated, Multi Supply Voltage, Power Shut Off | 1.8V/ 1.2V ... 3.3V | standard speed & power, multivoltage, 1.8V, junction isolated |
| D_CELLSL_JIM3V | Multi Supply Voltage, Power Shut Off, Junction Isolated | 3.3V/ 1.8V ... 3.3V | standard speed & power, multivoltage, 3.3V, junction isolated |

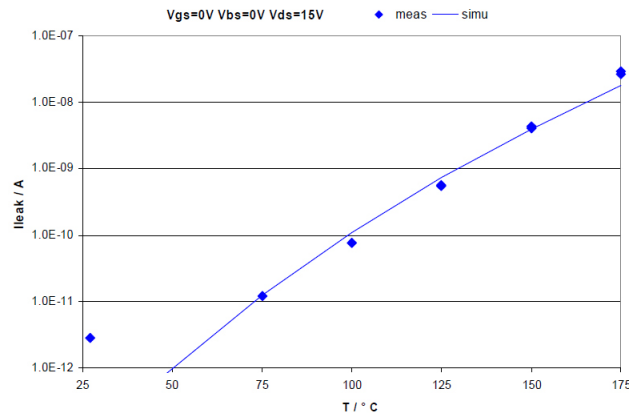
ANALOG LIBRARIES

| XH018 3.3V A_CELLS ANALOG LIBRARY | | | |
|-----------------------------------|--|---|--|
| Library | Cell Name | Operating conditions | Required module |
| Bias Cells | abiac01_3v3 abiac02_3v3 abiac03_3v3 | VDD: 2.7V to 3.6V; T: -40...125°C | LPMOS, MET3 |
| Bias Cells | acsoc01_3v3 acsoc02_3v3 | VDD: 2.7V to 3.6V; T: -40...125°C | LPMOS, MET3 |
| Bandgap | abgpc01_3v3 abgpc02_3v3 abgpc04_3v3 | VDD: 2.4V to 3.6V; T: -40...125°C | LPMOS, MET3 |
| Bandgap | abgpc03_3v3_ji | VDD: 2.1V to 3.6V; T: -40...150°C | LPMOS, ISOMOS, HVMOS, DEPL, MIM-MET3, METMID |
| Operational Amplifier | aopac01_3v3 aopac02_3v3 aopac03_3v3 aopac04_3v3 | VDD: 2.7V to 3.6V; T: -40...85°C | LPMOS, MET3 |
| Comparators | acmpc01_3v3 acmpc02_3v3 acmpc03_3v3 | VDD: 2.7V to 3.6V; T: -40...85°C | LPMOS, MET3 |
| RC Oscillators | arcoc01_3v3 arcoc02_3v3 arcoc03_3v3 arcoc04_3v3 | VDD: 2.7V to 3.6V; T: -40...125°C | LPMOS, MET3 |
| RC Oscillators | arcoc01_3v3_ji | VDDA: 2.2V to 3.6V; VDD: 1.62V to 1.98V; T: -40...125°C | LPMOS, ISOMOS, MET3, METMID, MIM |
| RC Oscillators | arcoc03_3v3_ji | VDDA: 3.0V to 3.6V; VDD: 1.5V to 1.98V; T: -40...150°C | LPMOS, ISOMOS, MET3, METMID, MIM |
| Crystal Oscillators | axtoc01_3v3_ji axtoc02_3v3_ji | VDD: 2.4V to 3.6V; T: -40...85°C | LPMOS, MET3, METMID |
| ADC | aadcc01_3v3 aadcc01_3v3_ji | VDDA: 2.7V to 3.6V; T: -40...85°C | LPMOS, MET3, METMID, MIM LPMOS, ISOMOS, MET3, METMID, MIM |
| DAC | adacc01_3v3 adacc01_3v3_ji | VDDA: 2.7V to 3.6V; T: -40...85°C | LPMOS, MET3 LPMOS, ISOMOS, MET3 |
| Power-On-Reset | aporc02_3v3 aporc03_3v3 | VDD: 2.7V to 3.6V; T: -40...85°C | LPMOS, MET3 |
| Voltage Regulators | aregc01_3v3 | T: -40...85°C | LPMOS, MET3, METMID |
| Over-Temperature Detector | atmpc01_3v3 | VDD: 2.7V to 3.6V; T: -40...140°C | LPMOS, MET3 |

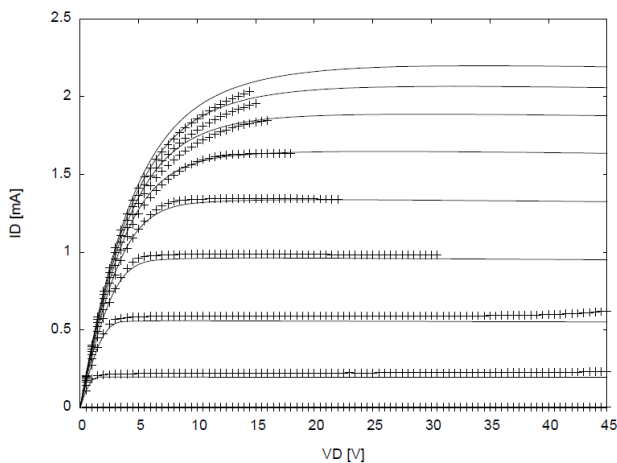
EXAMPLES FOR MEASURED AND MODELED PARAMETER CHARACTERISTICS



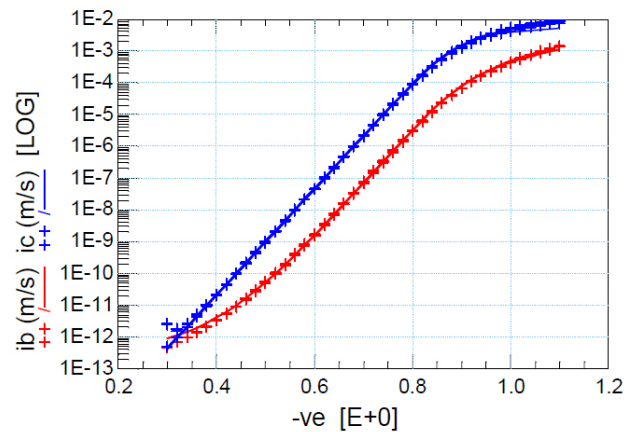
Output characteristics of device ne for a typical wafer, $W/L = 10/0.18$, $V_{GS} = 0.4, 0.75, 1.10, 1.45, 1.80V$, $V_{BS} = 0V$ symbol = measured, solid line = BSIM3V3 model



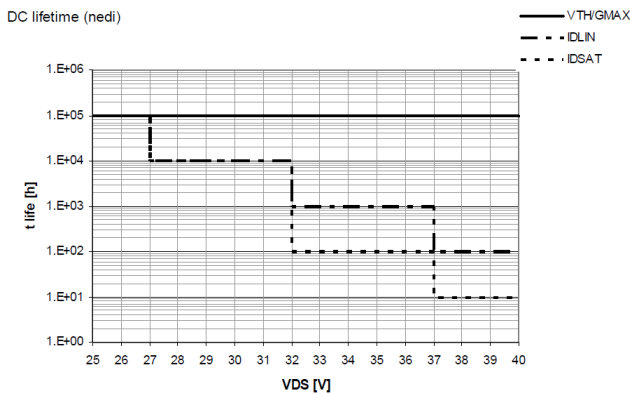
Leakage current vs. $1/T$ of device ned1 for a typical wafer. $W/L = 100/0.65$, $V_{GS} = V_{BS} = 0V$, symbol = measured, solid line = BSIM3V3 subcircuit model



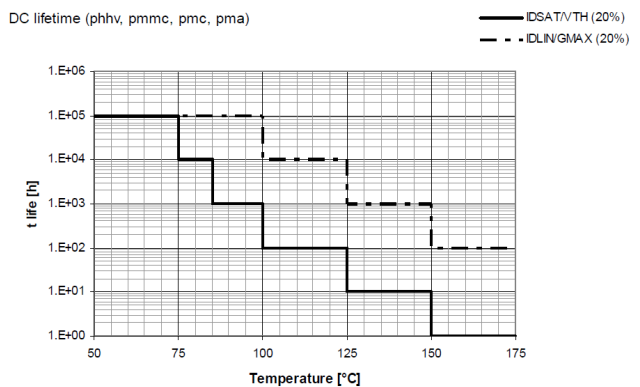
Output characteristics of device ped for a typical wafer. $W/L = 20/5$, $V_{GS} = 2, 4, 6, 8, 10, 12, 14, 16, 18V$, $V_S = V_B = 0V$, symbol = measured, line = HiSIM_HV



Gummel plot of 3.3V vertical HV NPN transistor qnva for a typical wafer, Emitter length $3.0 \mu m$, $V_{CB} = 1, 2, 3V$, symbols = measured values, solid line = VBIC model

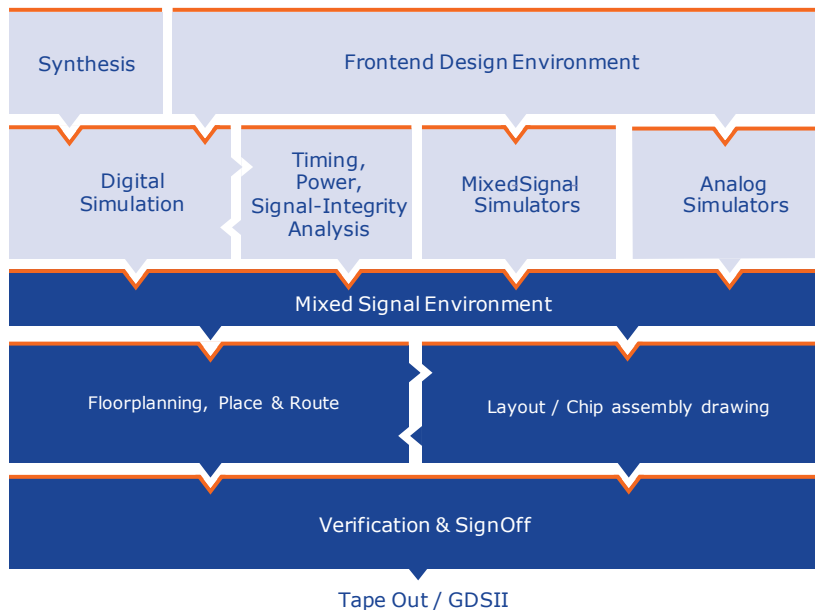


Hot Carrier Injection plot for device ned1 for a typical wafer.



Negative Bias Temperature Instability plot for device phhv for a typical wafer.

XH018 SUPPORTED EDA TOOLS



Note: Diagram shows overview of reference flow at X-FAB. Detailed information of supported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center X-TIC.

X-FAB'S IC DEVELOPMENT KIT "THEKIT"

The X-FAB IC Development Kit is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard EDA tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries

which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well. The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

CONTACT

Marketing & Sales Headquarters
 X-FAB Semiconductor Foundries AG
 Haarbergstr. 67, 99097 Erfurt, Germany
 Tel.: 49-361-427 6160
 Fax: 49-361-427 6161
 Email: info@xfab.com
 Web: http://www.xfab.com

Technology & Design Support
 hotline@xfab.com
 Silicon Foundry Services
 sifo@xfab.com

DISCLAIMER

Products sold by X-FAB are covered by the warranty provisions appearing in its Term of Sale. X-FAB makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. X-FAB reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with X-FAB for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as medical life-support or life-sustaining equipment are specifically not recom-

mended without additional processing by X-FAB for each application. The information furnished by X-FAB is believed to be correct and accurate. However, X-FAB shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interrupt of business or indirect, special incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of X-FAB's rendering of technical or other services.
 © 2017 by X-FAB Semiconductor Foundries AG. All rights reserved.