

# 0.13 µm Process Family:

## > XC013



### 0.13 Micron Modular CMOS Analog Mixed Signal Technology

#### DESCRIPTION

The XC013 series is X-FAB's 0.13 micrometer mixed-signal CMOS technology. This single poly 0.13 micrometer process with up to six metal layers is well-suited for highly integrated mixed-signal System-on-Chip applications addressing the communications, consumer or industrial market.

The modular process concept allows for a high flexibility in analog and mixed-signal designs. Comprehensive design rules, precise SPICE models, analog and digital libraries, IPs and development kits support the process on platforms supplied by the major EDA tool vendors.

#### KEY FEATURES OVERVIEW

- 0.13-micron single poly, N-well CMOS basic process
- Easy shrink from 0.18µm
- Modular concept, 8" wafers
- Optional 3.3V module
- Isolation well for all 1.5V and 3.3V MOS devices
- Up to six AL-based metal layers
- Metal-Insulator-Metal capacitors
- High resistive poly resistors
- One-Time programmable memory module for trimming and data storage
- Operating Conditions:  $T_j = -40^{\circ}\text{C} \dots +125^{\circ}\text{C}$
- Common-Timing-Engine in Cadence P&R encounter platform
- Cadence & Mentor Graphic PDK

#### APPLICATIONS

- Mixed-signal embedded systems / systems-on-chip (SOC)
- Low power mixed-signal circuits
- High Precision mixed-signal circuits

#### QUALITY ASSURANCE

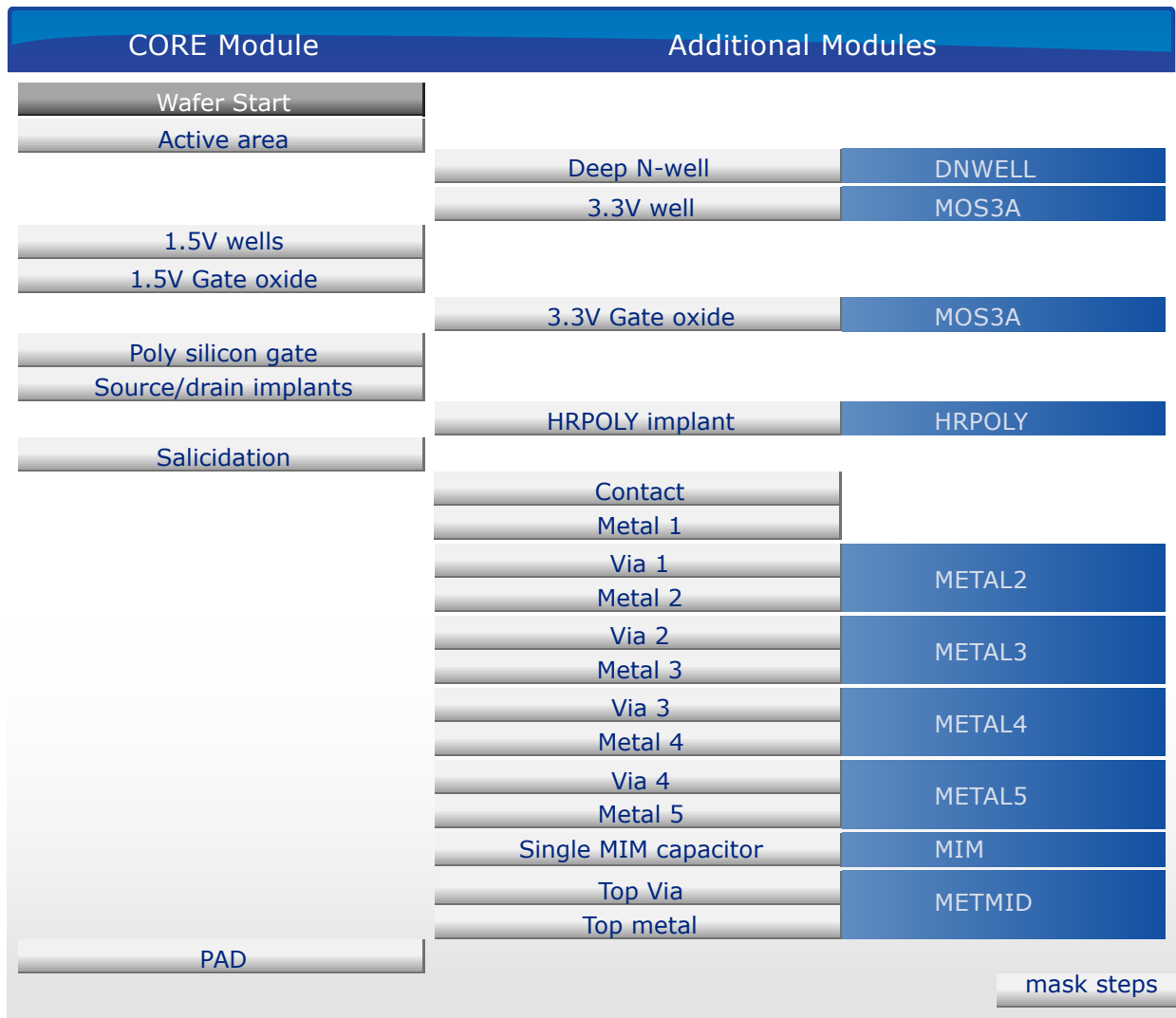
X-FAB spends a lot of effort to improve the product quality and reliability and to provide comprehensive support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by

strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, ISO TS 16949 and other standards.

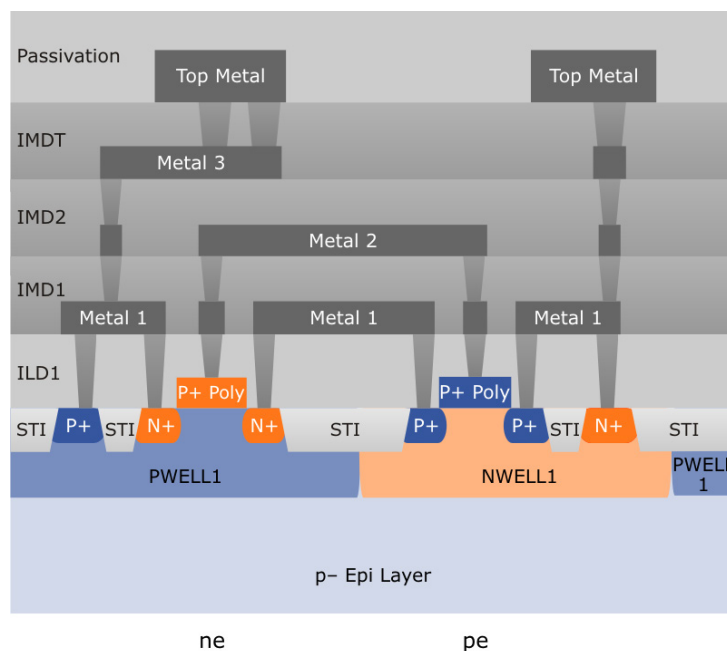
#### DELIVERABLES

- PCM tested wafers
- Optional engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional design services: feasibility studies, Place & Route, synthesis, custom block development

XCO13 PROCESS FLOW



XCO13 DEVICES SCHEMATIC CROSS SECTION



### XC013 CORE MODULE

Module Name	Descriptions	Masks No.
MOSLP	1.5V Low Power MOS module	11

### XC013 ADDITIONAL MODULES

Module Name	Descriptions	Masks No.
MOS3A	3.3V CMOS module	5
HRPOLY	High resistance polysilicon module	1
ISOMOS	Triple well isolated CMOS module	1
MIM	Single MIM capacitor module	1
METAL1	Metal 1 module	2
METAL2	Metal 2 module	2
METAL3	Metal 3 module	2
METAL4	Metal 4 module	2
METAL5	Metal 5 module	2
METMID	Top metal module	2
OTP	One-Time Programmable memory module	0

### XC013 RESTRICTION FOR MODULE COMBINATIONS

Module name	Use of the module also requires use of the following module(s)	Use of the module is not available with the use of the following module(s)
MOSLP	METAL1+ METAL2+METAL3+METMID	
MIM	METMID	
METAL3	METAL1+METAL2	
METAL4	METAL3	
METAL5	METAL4	

### XC013 BASIC DESIGN RULES

Mask	width [ $\mu\text{m}$ ]	Spacing [ $\mu\text{m}$ ]
N-well	0.6	0.6
Active Area	0.15	0.21
Poly-silicon Gate/Resistor	0.13	0.18
Contact	0.16	0.18
Metal 1	0.16	0.18
Via 1...4 / Metal 2...5	0.19 / 0.20	0.22 / 0.21
Via TP / Metal top	0.36 / 0.44	0.35 / 0.46

### XC013 METAL OPTIONS

Number of Metals	Available Metal Layer Combinations	Module Names
4	MET1 - MET2 - MET3 - METTP	MOSLP+METAL1+METAL2+METAL3+METMID
5	MET1 - MET2 - MET3 - MET4 - METTP	MOSLP+METAL1+METAL2+METAL3+METAL4+METMID
6	MET1 - MET2 - MET3 - MET4 - MET5 - METTP	MOSLP+METAL1+METAL2+METAL3+METAL4+METAL5+METMID

## Active Devices

### XC013 MOS LOW VOLTAGE TRANSISTORS

Device	Name	Available with module	VT  [V]	IDS [ $\mu\text{A}/\mu\text{m}$ ]	IOFF [ $\text{pA}/\mu\text{m}$ ]	BVDS [V]	Max. VDS [V]	Max. VGS [V]
1.5V native NMOS	nn	MOSLP	0.24	270				
1.5V LP NMOS	ne	MOSLP	0.54	455	< 30	> 2.5	1.65	1.65
1.5V LP PMOS	pe, pe_5	MOSLP	0.59	190	< 30	> 2.5	1.65	1.65
3.3V native NMOS	nn3	MOS3A	0.1	358				
3.3V NMOS	ne3	MOS3A	0.72	544	< 10	> 5.5	3.6	3.6
3.3V PMOS	pe3, pe3_5	MOS3A	0.65	330	< 10	> 5.5	3.6	3.6

### XC013 ISOMOS TRANSISTORS

Device	Name	Available with module	VT  [V]	IDS [ $\mu\text{A}/\mu\text{m}$ ]	IOFF [ $\text{pA}/\mu\text{m}$ ]	BVDS  [V]	max. VDS [V]
Iso. 1.5V LP NMOS	nei, nei_6	ISOMOS	0.54	465	< 30	> 2.5	1.65
Iso. 1.5V LP PMOS	pei, pei_5	ISOMOS	0.59	190	< 30	> 2.5	1.65
Iso3.3V NMOS	ne3i, ne3i_6	MOS3A+ISOMOS	0.72	544	< 10	> 5.5	3.6
Iso. 3.3V PMOS	pe3i, pe3i_5	MOS3A+ISOMOS	0.65	330	< 10	> 5.5	3.6

### XC013 BIPOLAR TRANSISTORS

Device	Name	Available	BETA	VA [V]	BVCEO [V]	VBE [mV]	max. VCE [V]
3.3V vPNP	qpva3/b3/c3 *	MOS3A	4.8/4.6/4.5	> 100		705/665/630	3.6
3.3V vNPN	qnva3	MOS3A+ISOMOS	9.1	76	> 13	710	3.6

\* devices with emitter area =  $2 \times 2 \mu\text{m}^2$  /  $5 \times 5 \mu\text{m}^2$  /  $10 \times 10 \mu\text{m}^2$

## Passive Devices

### XC013 MIM CAPACITORS

Device	Name	Available	Area Cap [ $\text{fF}/\mu\text{m}^2$ ]	Voltage Coeff. [ppm/V]	Temp. Coeff. [ $10^{-6}/\text{K}$ ]	BV  [V]	max. VTB [V]
M3/MTP MIM M4/MTP MIM M5/MTP MIM	cmm4t, cmm5t, cmm6t	MIM	1	14.12	38.9	> 20	3.6

### XC013 POLY RESISTORS

Device	Name	Available with module	RS [ $\Omega/\square$ ]	Temp. Coeff. [ $10^{-3}/\text{K}$ ]	Max VTB [V]
N+ Poly	rnp1, rnp1_3*	MOSLP	184	-0.14	3.6
P+ Poly	rpp1, rpp1_3*	MOSLP	260	0.005	3.6
P+ Poly silicided	rpp1s, rpp1s_3*	MOSLP	6.6	2.97	3.6
P- Poly	rpp1k1, rpp1k1_3*	HRPOLY	990	-0.89	3.6

\* These devices are variants of the corresponding basic device with an underlying well, but not crossing a well boundary. The models realise an improved description of bulk voltage dependency. Parameters of these devices are identical to the corresponding basic device.

**Passive Devices (Continued)**

XC013 DIFFUSION RESISTORS						
Device	Name	Available with module	RS [ $\Omega/\square$ ]	Thickness/junc. depth [ $\mu\text{m}$ ]	Temp. Coeff. [ $10^{-3}/\text{K}$ ]	Max VTB [V]
1.5V N+ diffusion	rdn	MOSLP	77	0.23	1.47	1.65
1.5V N+ diffusion silicided	rdns	MOSLP	6		3.07	1.65
1.5V P+ diffusion	rdp	MOSLP	81	0.225	1.47	1.65
1.5V P+ diffusion silicided	rdps	MOSLP	6		2.95	1.65
1.5V N-well	rnw	MOSLP	985	1.7	3.06	1.65
3.3V N+ diffusion	rdn3	MOS3A	73		1.44	3.6
3.3V N+ diffusion silicided	rdn3s	MOS3A	6		3.11	3.6
3.3V P+ diffusion	rdp3	MOS3A	83		1.45	3.6
3.3V P+ diffusion silicided	rdp3s	MOS3A	6		3.11	3.6
3.3V N-well	rnw3	MOS3A	1140	2.5	3.6	3.6
DN-well	rdnw	ISOMOS	1600	3.5	5.9	3.6

XC013 METAL RESISTORS							
Device	Name	Available with module	RS [ $\Omega/\square$ ]	Thickness/junc. depth [ $\mu\text{m}$ ]	Max J/W [ $\text{mA}/\mu\text{m}$ ]	Temp. Coeff. [ $10^{-3}/\text{K}$ ]	Max VTB [V]
Metal 1	rm1	MOSLP	0.23	0.295	0.18	2.91	3.6
Metal 2	rm2	METAL2	0.095	0.475	0.8	3.05	3.6
Metal 3	rm3	METAL3	0.095	0.475	0.8	3.43	3.6
Metal 4	rm4	METAL4	0.095	0.475	0.8	3.43	3.6
Metal 5	rm5	METAL5	0.095	0.475	0.8	3.43	3.6
Top Metal	rmtp	METMID	0.035	3.04	1.6	4	3.6

XC013 DIFFUSION DIODES						
Device	Name	Available with module	Area Cap [ $\text{fF}/\mu\text{m}^2$ ]	BV  [V]	Leakage Current [ $\text{fA}/\mu\text{m}^2$ ]	Max VCC [V]
N+ diif. /Psub	dnat	MOSLP	0.137	> 5.5	$2.5 \times 10^{-2}$	1.65
1.5V N+ diff. / PW	dn	MOSLP	0.922	> 5.5	1.5	1.65
1.5V P+ diff. /NW	dp	MOSLP	1.205	> 5.5	$6.8 \times 10^{-4}$	1.65
1.5V NW /Psub	dnw	MOSLP	0.126	> 9	$2.0 \times 10^{-3}$	3.6
3.3V N+ diff. /PW	dn3	MOS3A	1.013	> 5.5	$9.3 \times 10^{-2}$	3.6
3.3V P+ diff. /NW	dp3	MOS3A	1.052	> 5.5	$3.53 \times 10^{-5}$	3.6
3.3V NW /Psub	dnw3	MOS3A	0.127	> 9	$3.71 \times 10^{-4}$	3.6
1.5V P+ diff. /DNW	dpdnw	ISOMOS	0.577	> 5.5	$5.7 \times 10^{-5}$	1.65
PW /DNW	dpw	ISOMOS	0.268	> 9	$7.16 \times 10^{-5}$	3.6
3.3V PW /DNW	dpw3	MOS3A+ISOMOS	0.284	> 9	$9.16 \times 10^{-5}$	3.6
DNW /Psub	ddnw	ISOMOS	0.111	> 9	$2.0 \times 10^{-3}$	3.6

## STANDARD CELLS LIBRARIES

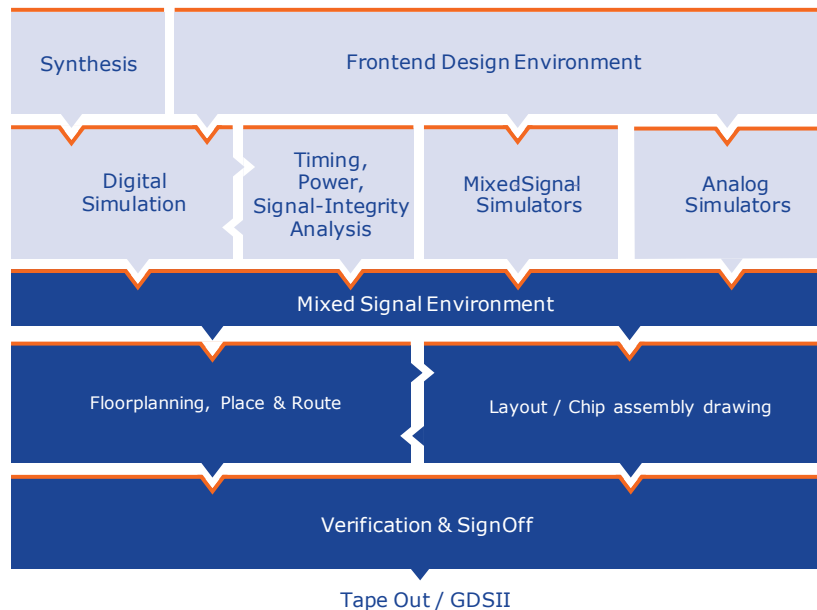
XC013 STD CELLS LIBRARY			
Device	Library feature	Voltage range	Application benefits
D_CELLS_JI	Junction Isolated, Standard Speed & Low Power	1.5V	standard speed, low power cells (X0) available, noise protection, voltage shifting

## I/O LIBRARIES

XC013 I/O CELLS LIBRARY					
Device	Library Feature	V <sub>CORE</sub> *	V <sub>IO</sub> *	ESD Level	Application benefits
IO_CELLS_3V	Standard, 1.5V/3.3V multi supply voltage	1.5V	3.3V	2kV HBM	Pad limited
IO_CELLS_F3V	Standard, 1.5V/3.3V multi supply voltage	1.5V	3.3V	2kV HBM	Core limited
IO_CELLS_C1V5	Standard, V <sub>CORE</sub> =V <sub>IO</sub> single supply voltage	1.5V	1.5V	2kV HBM	Pad limited
IO_CELLS_FC1V5	Standard, V <sub>CORE</sub> =V <sub>IO</sub> single supply voltage	1.5V	1.5V	2kV HBM	Core limited
IO_CELLS_C3V	Standard, V <sub>CORE</sub> =V <sub>IO</sub> single supply voltage	3.3V/2.2V	3.3V/2.2V	2kV HBM	Pad limited
IO_CELLS_FC3V	Standard, V <sub>CORE</sub> =V <sub>IO</sub> single supply voltage	3.3V/2.2V	3.3V/2.2V	2kV HBM	Core limited

\* Please refer to the library databook for details about available PVT ranges

**XC013 SUPPORTED EDA TOOLS**



Note: Diagram shows overview of reference flow at X-FAB. Detailed information of supported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center X-TIC.

**X-FAB'S IC DEVELOPMENT KIT "THEKIT"**

The X-FAB IC Development Kit is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries

which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well. The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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