0.35 µm Process Family:

XA035

0.35 Micron High Temperature Modular CMOS Technology

MIXED-SIGNAL FOUNDRY EXPERTS

DESCRIPTION

The XA035 Series is X-FAB's 0.35 Micron High Temperature CMOS Technology. Main target applications are high temperature automotive and Industrial products with temperature range up to 175°C. All modules are comparable in Design Rules and Transistor Performance with our corporate state of the art 0.35 µm CMOS Processes. Comprehensive design rules, precise SPICE models, analog and digital libraries, IP's and development kits support the process on platforms supplied by the major EDA tool vendors.

KEY FEATURES OVERVIEW

- 0.35-micron single poly, triple metal N-well CMOS basic process
- 3.3V logic layout & performance compatible with XH035 as well as the industry standard
- Extended high temperature characterisation
- **NEW:** Improved ESD robust devices
- Device model improvement for high temperature environment
- Process Reliability document.
- Lifetime Calculator tool for device reliability estimation based on automotive mission profile.
- Up to 175°C operating temperature, extending beyond AEC Q100 requirement.
- High Density up to 18000 gates per mm^2
- I/O cell library with 4kV HBM ESD protection levels
- Typical and worst-case models - BSIM3v3.24 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterised & included in model
- Interconnect model-Diva 2.5D
- RF characterisation and models for all RF MOS transistors and passive components
- Comprehensive PDK support for Cadence, Mentor, Synopsys and Tanner

APPLICATIONS

- Mixed-signal embedded systems / systems-on-chip (SOC)
- High Precision mixed-signal circuits
- Analog frontends for sensors
- RF applications
- Communications, consumer, automotive and industrial markets

QUALITY ASSURANCE

X-FAB spends a lot of effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, ISO TS 16949 and other standards.

DELIVERABLES

- PCM tested wafers
- Optional production services: wafer sort
- Optional engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional design services: feasibility studies, Place & Route, synthesis, custom block development

DIGITAL LIBRARIES

- Foundry-specific optimized libraries
- Standard core library for high speed digital blocks
- Pad-limited IO library
- Core-limited IO library
- IEEE 1364 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models
- Synthesis libraries
- Macrofunction and IPs on request
- RAM, DPRAM, ROM

PRIMITIVE DEVICES

- NMOS/PMOS transistors
- Bipolar transistors
- Diodes
- Capacitors
- Resistors
- Inductors
- Varactors

XA035 CORE MODULE

Module Name	Descriptions	Masks No.
MOS	Core MOS module	14

XA035 ADDITIONAL MODULES

Module Name	Descriptions	Masks No.
MOS5A	Mid gate oxide module	3
ISOMOS	Isolated MOS module	2
THKOX	Thick Gate oxide module	3
HVMOSMID	Mid gate oxide module for HV	3
HVMOSTHK	Thick gate oxide module for HV	3
NHVEMID	Mid gate oxide module for high voltage transistors	3
NHVETHK	Thick gate oxide module for high voltage transistors	3
PHVEMID	Mid gate oxide module for high voltage transistors	1
PHVETHK	Thick gate oxide module for high voltage transistors	1
DEPL	Depletion NMOS module	1
BURDIF	Buried N module	1
CAPPOLY	Polysilicon 2 module	1
HRPOLY	High resistance polysilicon	1
XRPOLY	Very high resistance polysilicon	1
TEEPROM	EEPROM module	0
CEEPROM	EEPROM module	0
MIM	MIM capacitor module	1
DMIM	Double MIM module	1
METAL2	Top metal 2 module	-2
METAL4	Metal 4 module	2
THKMET3	Thick metal 3 module	0
THKMET	Thick metal 4 module	2
PIMIDE	Polyimide module	1

XA035 ADDITIONAL MASK COUNT FOR MODULES COMBINATION

Module Name	When combines with modules	Combined additional mask count
THKOX	ISOMOS	4
HVMOSMID	MOS5A	5
HVMOSTHK	THKOX	5
NHVEMID	MOS5A or HVMOSMID	5
PHVEMID	HVMOSMID	2
NHVETHK	THKOX	4
NHVETHK	HVMOSTHK	5
PHVETHK	HVMOSTHK	2

XA035 RESTRICTIONS FOR MODULE COMBINATIONS

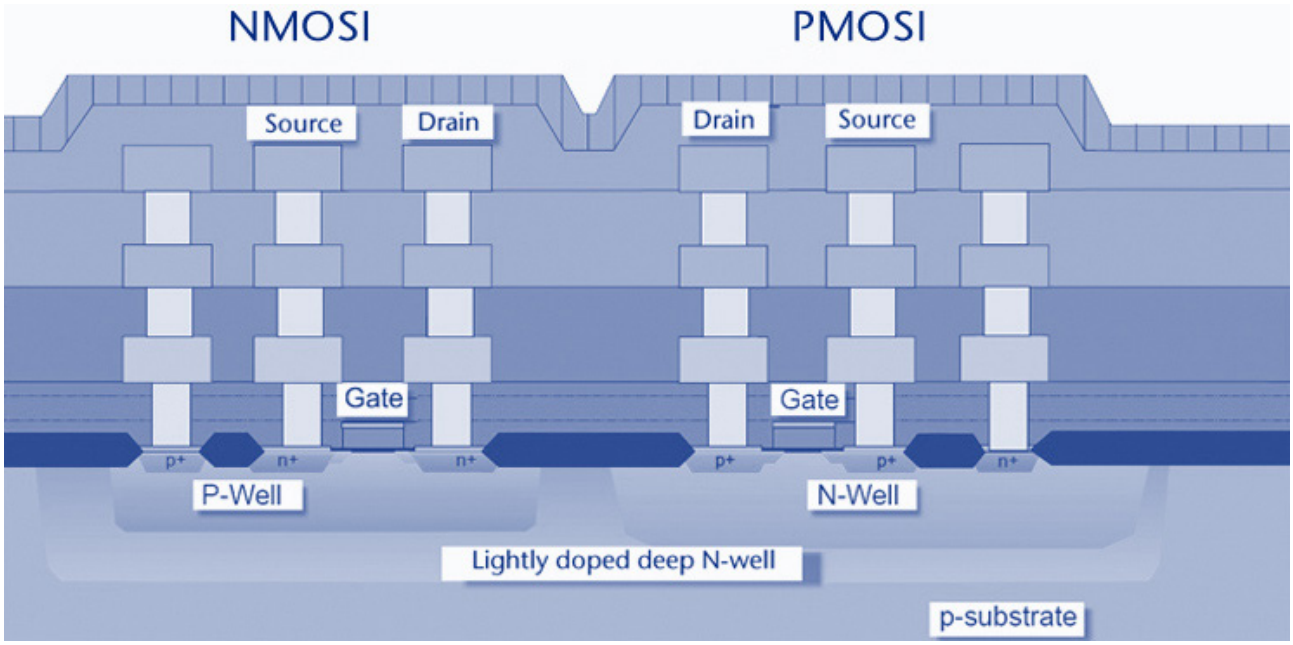
Module name	Use of the module also requires use of the following module(s)	Use of the module is not available with the use of the following module(s)
MOS5A		THKOX, HVMOSTHK, NHVETHK, PHVETHK
THKOX		MOS5A, HVMOSMID, NHVEMID, PHVEMID
HVMOSMID	ISOMOS	THKOX, HVMOSTHK, NHVETHK, PHVETHK
HVMOSTHK	ISOMOS	MOS5A, HVMOSMID, NHVEMID, PHVEMID
NHVEMID	ISOMOS	THKOX, HVMOSTHK, NHVETHK, PHVETHK
PHVEMID	NHVEMID	THKOX, HVMOSTHK, NHVETHK, PHVETHK
NHVETHK	ISOMOS	MOS5A, HVMOSMID, NHVEMID, PHVEMID
PHVETHK	NHVETHK	MOS5A, HVMOSMID, NHVEMID, PHVEMID
DEPL	THKOX	
XRPOLY	HRPOLY	
TEEPROM	THKOX, BURDIF	METAL2*
MIM		DMIM, METAL2
DMIM	METAL4 or THKMET	MIM, METAL2
METAL2		MIM, DMIM, TEEPROM, NHVEMID, NHVETHK, PHVEMID, PHVETHK, METAL4, THKMET3, THKMET
METAL4		METAL2, THKMET3, THKMET
THKMET3		DMIM, TEEPROM, METAL2, METAL4, THKMET
THKMET		METAL2, METAL4, THKMET3

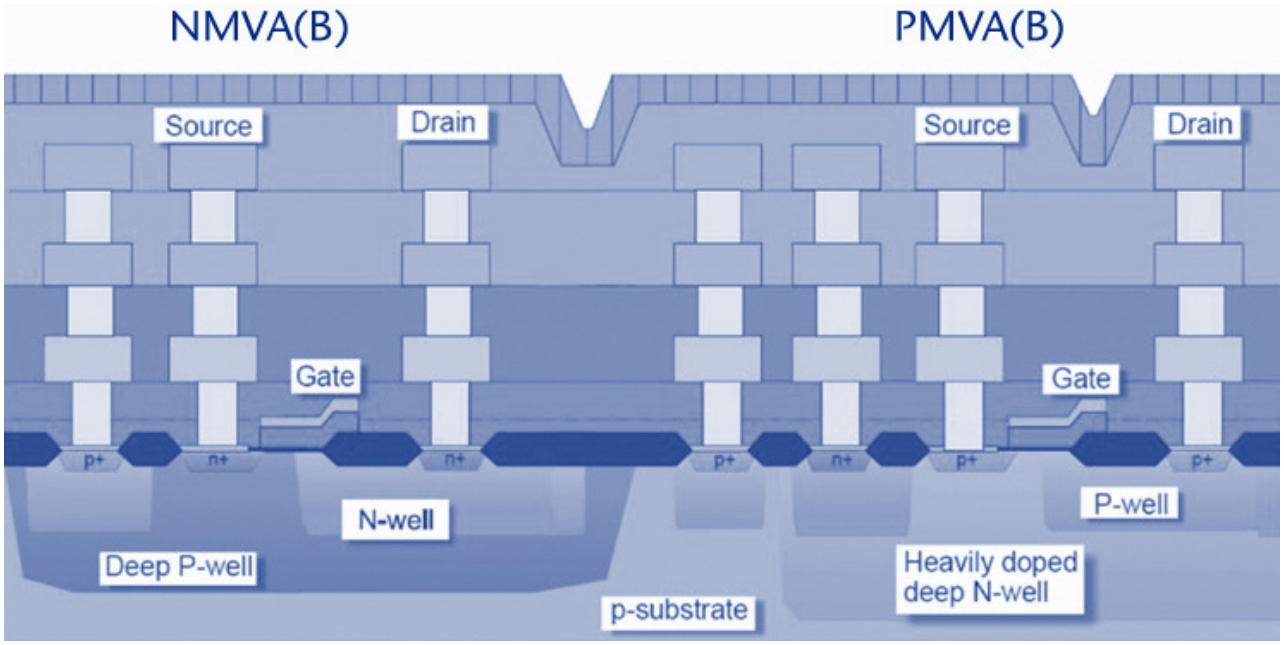
* The TEEPROM module is not allowed with METAL2 only because TEEPROM blocks require three metal layers.

XA035 BASIC DESIGN RULES

Mask	width [µm]	Spacing [µm]
N-well	1.6	1.0
Active area	0.5	0.6
Poly-silicon gate /resistor	0.35	0.45
Contact	0.4	0.4
Metal 1	0.5	0.45
Via 1 /2 /3	0.5	0.45
Metal 2 /3	0.6	0.5(0.6 if top layer)
Metal 4 / Thick Metal 4	0.6 / 3.0	0.69 / 2.50

XA035 DEVICES SCHEMATIC CROSS SECTION





XA035 PROCESS FLOW

Core Module	Additional Modules	
Zero Layer		T/CEEPROM
	DW implant	HVMOS(MID/THK)
	DW implant	NHVE(MID/THK)
	DW implant	ISOMOS
	HDW implant	THKOX
	DS implant	ISOMOS/THKOX
	DW implant	PHVE(MID/THK)/ HVMOS(MID/THK)
Active area		
	BN implant	BURDIF
N-well		
P-well		
	ESD P-well implant	NHVE(MID/THK)
	VP implant	THKOX
	ND implant	DEPL
	Dual gate oxide	MOS5A/THKOX/ NHVE/HVMOS
	High res. poly	HRPOLY
Poly 1		
	5V N- Implant	MOS5A
N- implant		
P- implant		
	Poly 2	CAPPOLY
N+ implant		
P+ implant		
	Very high res. poly	XRPOLY
Silicide block		
Contact		
	DMIM capacitor	DMIM
Metal 1		
Via 1		
	MIM capacitor	MIM
Metal 2		
Via 2	Not available with METAL2	THKMET3
	DMIM capacitor	DMIM
Metal 3	Not available with METAL2	THKMET3
	Via 3	METAL4/THKMET
	Metal 4	
PAD	Polyimide deposition	PIMIDE
Back side grinding		mask steps

Active Devices

XA035 MOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	|BVDS| [V]	max. |VDS| [V]	max. |VGS| [V]
3.3V NMOS	nmos	MOS	0.6	500	> 5.5	3.6	3.6
3.3V PMOS	pmos	MOS	0.74	250	> 5.5	3.6	3.6
5V NMOS (mid oxide)	nmos5	MOS5A	0.95	450	> 7	5.5	5.5
5V PMOS (mid oxide)	pmos5	MOS5A	0.94	205	> 7	5.5	5.5
5V NMOS (thick oxide)	nmv	THKOX	1.15	150	> 8	5.5	5.5
5V PMOS (thick oxide)	pmv	THKOX	0.95	76	> 8	5.5	5.5
5V Native NMOS (thick oxide)	nnmv	THKOX	0.04	220	> 8	5.5	5.5
5V PMOS HV iso. (thick oxide)	pmvic	NHVETHK	1.62	57	> 8	5.5	5.5

XA035 ISOMOS TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	|BVDS| [V]	max. |VDS| [V]	max. |VGS| [V]
3.3V isolated NMOS	nmosi	ISOMOS	0.59	500	> 5	3.6	3.6
3.3V isolated PMOS	pmosi	ISOMOS	0.78	240	> 5	3.6	3.6
3.3V iso. PMOS, HV isolation	pmosib	ISOMOS	0.78	240	> 5	3.6	3.6
3.3V iso. NMOS, HV isolation	nmosia	HVMOSMID, HV-MOSTHK	0.58	500	> 5	3.6	3.6
3.3V iso. PMOS, HV isolation	pmosia	HVMOSMID, HV-MOSTHK	0.83	220	> 5	3.6	3.6
3.3V iso. NMOS, HV isolation	nmosic	NHVEMID, NHVETHK	0.54	540	> 5	3.6	3.6
3.3V iso PMOS, HV isolation	pmosic	NHVEMID, NHVETHK	0.81	240	> 5	3.6	3.6
5V iso. NMOS midox.	nmos5i	MOS5A+ISOMOS	0.91	465	> 7	5.5	5.5
5V iso. PMOS midox.	pmos5i	MOS5A+ISOMOS	1.01	190	> 7	5.5	5.5
5V iso. NMOS mid ox. HV iso.	nmos5ia	MOS5A+ISOMOS +HVMOSMID	0.88	420	> 7	5.5	5.5
5V iso. PMOS mid ox. HV iso.	pmos5ia	MOS5A+ISOMOS +HVMOSMID	1.1	175	> 7	5.5	5.5
5V iso. NMOS mid ox. HV iso.	nmos5ic	MOS5A+NHVEMID	0.9	465	> 7	5.5	5.5
5V iso. PMOS mid ox. HV iso.	pmos5ic	MOS5A+NHVEMID	1.05		> 7	5.5	5.5

XA035 ISOLATED HIGH VOLTAGE TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON [kΩ.µm]	BVDSS [V]	Max. |VGS| [V]
45V NDMOS with thin oxide	ndha	THKOX+ISOMOS	0.55	150	22	> 50	3.6
45V NDMOS with thick oxide	ndh	THKOX+ISOMOS	1.4	240	19.5	> 50	18

Active Devices *(Continued)*

XA035 HIGH VOLTAGE TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON [kΩ.µm]	RON.A [mΩ.mm²]	|BVDSS| [V]	Max. VGS [V]
45V drain NMOS	nhv	THKOX	0.9	320	15		> 50	18
45V drain PMOS	phv	THKOX	0.88	140	55		> 50	18
45V drain & source NMOS	nhhv	THKOX	0.97	155	33		> 50	18
45V drain & source PMOS	phhv	THKOX	0.97	54	130			18
45V (55V) drain compact PMOS	phva	HVMOSMID	1	110	44		> 55	5.5
40V compact NDMOS	ndhb	HVMOSMID	0.9	260	15		> 51	5.5
45V (55V) drain compact PMOS	phvb	HVMOSTHK	1.35	190	41		> 55	18
45V (55V) compact NDMOS	ndhc	HVMOSTHK	1.35	335	14		> 58	18
70V (75V) drain PMOS	phvc	HVMOSMID	1.12	85	59		> 85	5.5
70V (75V) compact NDMOS	ndhd	HVMOSMID	0.88	245	19		> 88	5.5
70V (75V) drain PMOS	phvd	HVMOSTHK	1.62	155	56		> 85	18
75V (75V) compact NDMOS	ndhe	HVMOSTHK	1.33	310	18		> 88	18
90V (100V) drain PMOS	phve	HVMOSMID	1.12	85	69		> 102	5.5
90V (100V) compact NDMOS	ndhf	HVMOSMID	0.88	245	21		> 110	5.5
90V (100V) drain PMOS	phvf	HVMOSTHK	1.6	150	64		> 105	18
90V (100V) compact NDMOS	ndhg	HVMOSTHK	1.33	310	19		> 110	18
20V compact NDMOS	ndhi	HVMOSTHK	1.3	420	9		> 30	18
55V drain NMOS in ESD Pwell mid oxide	nhvb1	NHVEMID	0.76	130	25	186	> 62	5.5
55V drain NMOS in ESD Pwell thick oxide	nhvc1	NHVETHK	1.65	200	40	142	> 62	18
75V drain NMOS in ESD Pwell mid oxide	nhvd1	NHVEMID	0.81	125	30	284	> 88	5.5
75V drain NMOS in ESD Pwell thick oxide	nhve1	NHVETHK	1.72	190	24	227	> 88	18
100V drain NMOS in ESD Pwell mid oxide	nhvf1	NHVEMID	0.83	125	32	334	> 110	5.5
100V drain NMOS in ESD Pwell thick oxide	nhvg1	NHVETHK	1.80	195	25	261	> 110	18
40V concentric NDMOS in ESD Pwell	ndhb1	NHVEMID	0.79	175	23	151	> 51	5.5
45V (55V) concentric NDMOS in ESD Pwell	ndhc1	NHVETHK	1.25	230	19	124	> 58	18
70V (75V) concentric NDMOS in ESD Pwell	ndhd1	NHVEMID	0.78	173	27	231	> 81	5.5
70V (75V) concentric NDMOS in ESD Pwell	ndhe1	NHVETHK	1.4	185	26	222	> 88	18
90V (100V) concentric NDMOS in ESD Pwell	ndhf1	NHVEMID	0.78	180	28	267	> 108	5.5
90V (100V) concentric NDMOS in ESD Pwell	ndhg1	NHVETHK	1.38	190	27	258	> 110	18

Active Devices *(Continued)*

XA035 MEDIUM VOLTAGE TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON [kΩ.µm]	|BVDS| [V]	max. |VDS| [V]	max. |VGS| [V]
12V drain NMOS (thin oxide)	nha	MOS	0.59	97	17	13.2	3.6	3.6
14V drain NMOS	nmvb	THKOX	0.97	340	9	> 20	14	18
14V drain & source NMOS	nmmvb	THKOX	0.92	300	11	> 20	14	18
14V drain PMOS	pmvb	THKOX	1.01	175	30	> 20	14	18
14V drain & source PMOS	pmmvb	THKOX	0.95	170	30	> 20	14	18
18V drain NMOS	nmva	THKOX	0.95	280	13	> 20	18	18
18V drain & source NMOS	nmmva	THKOX	0.94	250	15	> 20	18	18
18V drain PMOS	pmva	THKOX	1	185	30	> 20	18	18
18V drain & source PMOS	pmmva	THKOX	1	150	36	> 20	18	18

XA035 DEPLETION TRANSISTORS

Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	RON [kΩ.µm]	|BVDS| [V]	max. |VDS| [V]	max. |VGS| [V]
5V depletion NMOS	nmvd	DEPL	0.7	215		> 8	5.5	5.5
45V drain depletion NMOS	nhvd	DEPL	1.2	400	12	> 50	45	18
45V d & sdepletion NMOS	nhhvd	DEPL	1.1	180	31		45	18
90V (100V) concentric nDMOS	nddhg1	DEPL	still in development					

XA035 RF TRANSISTORS

Device	Name	Module	fT [GHz]	fmax [GHz]	max. |VDS| [V]	max. |VGS| [V]
3.3V PMOS for RF	nmosrf	MOS	25	40	3.6	3.6
3.3V NMOS for RF	pmosrf	MOS	15	24	3.6	3.6
3.3V isolated NMOS for RF	nmosirf	ISOMOS	25	40	3.6	3.6
3.3V isolated PMOS for RF	pmosirf	ISOMOS	15	24	3.6	3.6
5V NMOS with thick oxide for RF	nmvrf	THKOX	7	24	5.5	5.5
5V PMOS with thick oxide for RF	pmvrf	THKOX	4	15	5.5	5.5

XA035 BIPOLAR TRANSISTOR

Device	Name	Available	BETA	VA [V]	BVCEO [V]	VBE [mV]	max. VCE [V]
Vertical PNP	qp1/2/3/4	MOS	4.5	190	-	720	3.6
Lateral PNP	qpa	MOS	27	4.2	-	730	3.6
Vertical PNP	qpvh	THKOX	45	>70	> 110	695	100
Isolated Vertical NPN**	qnva, qnva2	THKOX	46	38	> 7	680	5.5
ESD protected HV PNP*	qpvhscr	PHVEMID, PHVETHK	2.3		> 90	537	80
Vertical PNP DPW	qpvha	THKOX	90	> 20	> 50	658	45
Iso. vNPN, octagonal**	qnvara/b/c	THKOX					5.5
Iso. vNPN, LDDNW collector	qnvb	ISOMOS	35	90	> 43	685	5.5
Iso. vNPN, LDDNW collector	qnvc	MOS5A+ISOMOS	55	55	> 41	680	5.5

* still in development
** qnva2 (two base stripes), qnvara (3.2µm² emitter), qnvarb, (11.5µm² emitter), qnvarc (44.1µm² emitter) are variants of qnva, refer to the device models for further details.

Passive Devices

XA035 DIFFUSION RESISTOR

Device	Name	Available with module	RS[Ω/□]	Thickness/junc. depth [µm]	Temp. Coeff. [10^{-3}/K]	Max |VTB| [V]
N+ diffusion	rdn, rdn_io*	MOS	85	0.17	1.5	6
N+ diff. in P-well/ LDD DNW	rdnlw, rdnlw_io*	ISOMOS	85	-	1.6	6
N+ diff. silicided	rsn	MOS	3.4	-	3.5	6
P+ diffusion	rdp, rdp_io*	MOS	150	0.21	1.44	6
P+ diff. in N-well/ LDD DNW	rdplw, rdplw_io*	ISOMOS	143	-	1.6	6
P+ diff. silicided	rsp	MOS	3.4	-	3.7	6
N-well	rw, rw_scr**	MOS	1160	1.1	3.9	6
Deep N-well	rhw	THKOX	1300	-	6.1	45
P+ diff.in heavily doped DNW	rdpmv_io*	THKOX	-	-	-	-
N+ diff. in deep P-well	rdnmv_io*	THKOX	-	-	-	-
N+ diff. in DPW, P-well	rdnmvwp_io*	THKOX	-	-	-	-
N+ diff. in DPW, ESD P-well	rdnmvep_io*	NHVEMID, NHVETHK	-	-	-	-
N+ diff. in P-well, ESD P-well	rdnep_io*	NHVEMID, NHVETHK	-	-	-	-

* These devices should be used only as ESD protection resistors in IO-cells
** This device is only intended for use in ESD protection structures

XA035 HIGH RESISTIVE RESISTORS

Device	Name	Available with module	RS [Ω/□]	Thickness/junc. depth [µm]	Max J/W [mA/µm]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
N+ Poly	rnp1	HRPOLY	1,000	0.30	2	-2.9	100
P+ Poly*	rpp1	HRPOLY	500	0.30	2	-0.61	100
Very high value Poly	rhp1	XRPOLY	10,000	-	-	-4.1	100

* Low TC Poly resistor

XA035 LOW TC RESISTORS

Device	Name	Available with module	RS [Ω/□]	Thickness/junc. depth [µm]	Max J/W [mA/µm]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
Low TC poly2	rzp2	CAPPOLY	200	0.25	2	-0.17	100
Poly 1 resistor	rp1	MOS	45	0.30	2	0.72	100
Poly 2 resistor	rp2	CAPPOLY	100	0.25	2	0.4	100
Poly 1 silicided	rsp1	MOS	4.5		2	3.4	100

Passive Devices *(Continued)*

XA035 METAL RESISTORS

Device	Name	Available with module	RS [Ω/□]	Thickness/junc. depth [µm]	Max J/W [mA/µm]	Temp. Coeff. [10^{-3}/K]	Max VTB [V]
Metal 1	rm1	MOS	0.090	0.58	1	3.4	100
Metal 2	rm2 rm2t	MOS METAL2	0.090 0.043	0.58 1.00	1 1.6	3.4	100
Metal 3	rm3t rm3 rm3l	MOS METAL4, THKMET THKMET3	0.043 0.090 0.012	1.00 0.58 2.90	1.6 1 6	3.4 3.4 3.5	100
Metal 4	rm4	METAL4	0.043	1.00	1.6	3.4	45
Thick Metal 4	rm4l	THKMET	0.012	2.90	6	3.5	45

XA035 POD CAPACITORS

Device	Name	Available with module	Area Cap [fF/µm²]	BV [V]	Perimeter Cap [fF/µm]	Max. VTB [V]
Poly on diffusion	cpod	BURDIF	3.9	> 5	0.2	18
Poly on diffusion	cpoda	BURDIF THKOX	3.9	> 5	0.2	18
Poly on diffusion (HV)	cpod_hv	BURDIF THKOX	0.85	> 35	0.12	20
Poly on diffusion (HDW)	cpodi_hv	BURDIF THKOX	0.85	> 35	0.12	45

XA035 PIP CAPACITORS

Device	Name	Available with module	Area Cap [fF/µm²]	BV [V]	V coef. [ppm/V]	Temp coef. [10^{-3}/K]	Max. VTB [V]
Poly1-Poly2	cpp	CAPPOLY	0.85	> 26	-120	0.023	100
Poly1- Poly2 (2T)	cpp2	CAPPOLY	0.85	> 26	-120	0.023	100

Note: For a high unit capacitance, the device cpp2 may be used in a stacked combination with other capacitors.

XA035 SANDWICH CAPACITORS

Device	Name	Available with module	Max VTB[V]	Cell Cap.[fF]
Poly 1/ Metal 1/ Metal 2/ Metal 3	csandwt	MOS	100	135
Poly 1/ Metal 1/ Metal 2/ Metal 3 Finger	csandwtf	MOS	100	255
Poly 1/Metal 1/Metal 2 / Metal 3/Metal 4	csandwtm	METAL4	100	294
Poly 1/ Metal 1/ Metal 2/ Metal 3/Metal 4	csandwtml	THKMET	100	277
Poly 1/ Metal 1/ Metal 2/ Thick Metal 3 Finger	csandwtfl	THKMET3	100	200

XA035 MIM CAPACITORS

Device	Name	Available	Area Cap [fF/µm²]	Voltage Coeff. [1/V]	Temp. Coeff. [ppm/K]	|BV|[V]	Max VTB [V]
MIM	cmm*	MIM	1.25	35	0.041	> 20	100
Double MIM	cdmm*	DMIM	2.5	35	0.041	> 20	100

*: These parameters are also valid for cmm2 and cdmm2 respectively.

Passive Devices *(Continued)*

XA035 STACKED CAPACITOR

Device	Available with module	Area Cap [fF/µm²]
cpp2 on cpoda	CAPPOLY+BURDIF+THKOX	4.6
cpp2 on cpod_hv (or cpodi_hv)	CAPPOLY+BURDIF+THKOX	1.6
cmm2 on cpp	MIM+CAPPOLY	2.0
cdmm2 on cpp	DMIM+CAPPOLY	2.6
cmm2 on cpod_hv (or cpodi_hv)	MIM+BURDIF+THKOX	2.0
cdmm2 on cpod_hv (or cpodi_hv)	DMIM+BURDIF+THKOX	2.6
cmm2 on cpp2 on cpod_hv (or cpodi_hv)	MIM+CAPPOLY+BURDIF+ THKOX	2.7
cdmm2 on cpp2 on cpod_h (or cpodi_hv)	DMIM+CAPPOLY+BURDIF+THKOX	3.4

XA035 MOS VARACTOR

Device	Name	Available with module	Tuning range [%]	Cap. @ +1V, 100 kHz [fF]	Cap. @ -1V, 100 kHz[fF]	Q factor @1GHz	Max. VGB [V]
MOS varactor	mosvc	MOS	71	3.5	1.0	50	3.6

XA035 DIODE VARACTOR

Device	Name	Available with module	Tuning range [%]	Q factor @1GHz	Cap. per length [fF/µm] @0V, 100kHz	Cap. per length [fF/µm] @2V, 100kHz	Max. |VCC| [V]
Diode varactor	dpvc	MOS	36	35	4.4	2.8	3.6

XA035 INDUCTOR

Device	Name	Module	No. of Turns	Outer Diameter [µm]	Inductance [nH]	Q-Factor
Asymmetric Thick Metal 4 Inductor	I09a	THKMET	6.5	280	10.2	6.4
Symmetric Thick Metal 4 Inductor	I09b	THKMET	6.5	280	9.6	5.6
Asymmetric Thick Metal 4 Inductor	I09c	THKMET3	6.5	280	9.8	5.8
Symmetric Thick Metal 4 Inductor	I09d	THKMET3	6.5	280	9.2	5.4

XA035 POLY DIODE

Device	Name	Available with module	Vforward [V]	Vreverse [V]	Max. VTB [V]
Polysilicon diode	dpol	XRPOLY	1.2	> 4	100

XA035 PROTECTION DIODE

Device	Name	Available with module	Leakage Current [pA/µm]	|BV|[V]	Max. |VCC| [V]
20V N-type Protection *	dnp20	ISOMOS	1000	25	30
30V N-type Protection *	dnp30	ISOMOS, THKOX	900	34	38
20V P-type Protection *	dpp20	ISOMOS	1250	26	31
30V P-type Protection	dpp30	THKOX	800	37	40

* Device not available with MOS5A, HVMOSMID, NHVEMID or PHVEMID modules

Passive Devices *(Continued)*

XA035 DIFFUSION DIODES

Device	Name	Available with module	Area junc. cap. [fF/µm²]	|BV| [V]	Max. |VCC| [V]	Area ILeak [fA/µm²]
N+ diffusion/ Pwell	dn	MOS	0.79	> 7	6	0.0004
N+ diffusion/ DPW	dnds	ISOMOS, THKOX	0.53	> 7	6	0.0004
P+ diffusion/ Nwell	dp, dp_scr	MOS	0.81	> 7	6	0.0005
P+ diff. (LDDNW)	dplw	ISOMOS	0.28	> 7	6	0.0005
P+ diffusion (HDDNW)	dphw	THKOX	0.36	> 7	6	0.0005
N-well/ DPW	dwds	ISOMOS, THKOX	0.39	> 21	18	0.0002
N-well	dw	MOS	0.12	> 7	6	0.0004
N-well (DW)	dwh	MOS	0.12	> 20	18	0.0004
P-well	dwplw	ISOMOS	0.24	> 12	10	0.0002
P-well (DW)	dwplwh	ISOMOS	0.24	> 45	40	0.0002
P-well (HDW)	dwphw	THKOX	0.3	> 30	30	0.0003
Deep P-well (HDW)	ddshw	THKOX	0.19	> 50	45	0.0003
Lightly doped N-well	dlw	ISOMOS	0.064	> 12	10	0.004
Heavily doped N-well	dhw	THKOX	0.094	> 20	18	0.0006
LDD N-well (HV)	dlwh, dlwhb*	ISOMOS	0.064	> 60 > 105	55 100	0.001
Heavily doped DNW	dhwh	THKOX	0.094	> 20	100	0.0006
P-well/ very lightly doped deep N-well	dwpvw	HVMOSMID, HVMOSTHK	0.25	> 50	45	0.0003
P-well/ medium doped deep N-well	dwplvw	HVMOSMID, HVMOSTHK	0.34	> 35	30	0.0005
HV deep P-well/ lightly doped deep N-well	dmplw	HVMOSMID, HVMOSTHK	0.216	> 65	55	0.0008
HV deep P-well/ Very lightly doped deep N-well	dmpvw, dmpvwh	HVMOSMID, HVMOSTHK	0.216	> 45 > 85	35 75	0.0006
HV deep P-well/ medium doped deep N-well	dmplvw	HVMOSMID, HVMOSTHK	0.33	> 35	30	0.0007
Medium doped deep N-well/ P-sub	dlvw	HVMOSMID, HVMOSTHK	0.14	> 110	100	0.0002
very lightly deoped deep N-well/ P-sub	dvw	HVMOSMID, HVMOSTHK	0.13	> 110	100	0.0002
ESD DNW /Psub	dclw	NHVEMID, NHVETHK	0.09	> 110	100	0.003
DPW/ ESD DNW	ddsclw	NHVEMID, NHVETHK	0.18	> 110	100	0.0035
ESD p-well/ ESD DNW	depclw	NHVEMID, NHVETHK	0.3	> 22	18	0.0025
(ESD)DPW/ ESD DNW	dsepclw	NHVEMIID, NHVETHK	0.19	> 110	100	0.003
HV DPW/ ESD DNW	dmpclw	PHVEMID, PHVETHK	0.23	> 37	25	0.00031
HV DPW/ CW	dmpcw	PHVEMID, PHVETHK	0.22	> 37	25	0.0003
P-well/ ESD DNW	dwplcw	NHVEMID, NHVETHK	0.3	> 25	18	0.0004

Note: These devices are only intended for the simulation of reverse leakage currents and junction capacitance. They must not be used in forward operation for normal operation modes. Please refer to the Process & Device Specification for more Diodes and details.
*dlwhb for use with pmosib, dsb1, dsb2 only

Passive Devices *(Continued)*

XA035 SCHOTTKY DIODES

Device	Name	Available with module	Vforward [V]	Leakage Current [nA]	|BV| [V]	Max. VTB [V]
Schottky HV isolation (thick oxide)	dsb1	ISOMOS+ (THKOX, HVMOSTHK, NHVETHK, PHVETHK)	0.04	55	> 22	100
Schottky HV isolation (mid oxide)	dsb2	ISOMOS+ (THKOX, HVMOSTHK, NHVETHK, PHVETHK)	0.04	75	> 22	100
Schottky HV isolation (thick oxide)	dsc1	NHVETHK	0.04	70	> 22	100
Schottky HV isolation (mid oxide)	dsc2	NHVEMID	0.04	75	> 22	100

Programmable Devices

XA035 OTP OVERVIEW

Type	Typical configuration	Typical Application
Poly Fuse	2 - 32 bits	Trimming
Zener Zap	2 - 32 bits	Trimming

XA035 ZENER ZAP DIODE

Device	Name	Avaialble with module	Vreverse [V] (unzap)	Vreverse [V] (zapped)	Max Iread [mA]
Zener Zap	dzap *	MOS	4	0.05	0.05
Zener zap (alignmnet insensitive)	dzapa *	MOS	4	0.05	0.05

* The zener zap diode, dzap/dzapa is only intended as a programmable element.

XA035 POLY FUSE

Device	Name	Available with module	Unprog. Res.[Ω]	Prog. Res.[kΩ]	Prog. Max VT1-T2 [V]	Unprog. Max VT1-T2 [V]
Poly Fuse	pfuse	MOS	16 ... 160	> 100	3.6	0.2

XA035 EEPROM

Parameter	Core EEPROM	Tiny EEPROM	Unit
Power supply in all modes	2.0 ... 3.6	1.8 ... 3.6	V
Data access time	max 150	max 250 @ VDD ≥2.0V	ns
Erase/Write pulse width	4 ... 8	4 ... 8	ms
Data retention	> 10 @ 85°C	> 10 @ 125°C	years
Number of erase/write Cycles @25°C	$1x10^5$	$1x10^5$	
Number of erase/write cycles @125°C	$1x10^4$	$1x10^4$ @ 150°C	
Temperature range in Read mode	-40 ... 175	-40 ... 175	°C
Temperature range in Erase/Write mode	-40 ... 175	-40 ... 155	°C

STANDARD CELLS LIBRARY

XA035 STD CELLS LIB

Device	Library feature	Voltage range	Application benefits
D_CELLS	Standard	3.3V	High speed
D_CELLSL	Low power	3.3V	Min. area, min. power consumption
D_CELLSL_HD	Low power, high density	3.3V	Min. area, min. power consumption, less noise
D_CELLSL_HDJI	Low power, high density, junction isolated	3.3V	Min. area, min. power consumption, min. noise

XA035 I/O CELLS LIBRARY

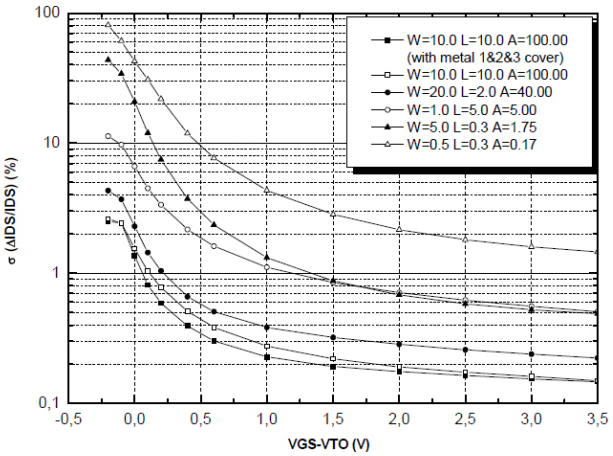
Device	Library Feature	V_{CORE}*	V_{IO}*	ESD Level**	Application benefits
IO_CELLS	Standard, V_{CORE}=V_{IO} single supply voltage	3.3V	3.3V	4kV HBM	Pad limited
IO_CELLS_F	Standard, V_{CORE}=V_{IO} single supply voltage	3.3V	3.3V	2kV HBM	Core limited
IO_CELLS_5V	Standard, $V_{CORE} \leq V_{IO}$ multi supply voltage	3.3V 3.3V 5.0V	3.3V 5.0V 5.0V	4kV HBM	Pad limited
IO_CELLS_F5V	Standard, $V_{CORE} \leq V_{IO}$ multi supply voltage	3.3V 3.3V 5.0V	3.3V 5.0V 5.0V	2kV HBM	Core limited
IO_CELLS_N5V	Standard, $V_{CORE} \leq V_{IO}$ multi supply voltage, ESD improved 5V nmos	3.3V 3.3V 5.0V	3.3V 5.0V 5.0V	4kV HBM	Pad limited
IO_CELLS_FN5V	Standard, $V_{CORE} \leq V_{IO}$ multi supply voltage, ESD improved 5V nmos	3.3V 3.3V 5.0V	3.3V 5.0V 5.0V	4kV HBM	Core limited
IO_CELLS_MV	Standard, 2.2V/3.3V multi supply voltage	2.2V	3.3V	4kV HBM	Pad limited
IO_CELLS_MVF	Standard, 2.2V/3.3V multi supply voltage	2.2V	3.3V	2kV HBM	Core limited
IO_CELLS_FE	Standard, $V_{CORE} \leq V_{IO}$ multi supply voltage	3.3V 2.2V 2.2V	3.3V 3.3V 2.2V	4kV HBM	Core limited

* Please refer to the library databook for details about available PVT ranges
** Refer to the library manual regarding the ESD Level of special I/O cells as 5V tolerant I/O's

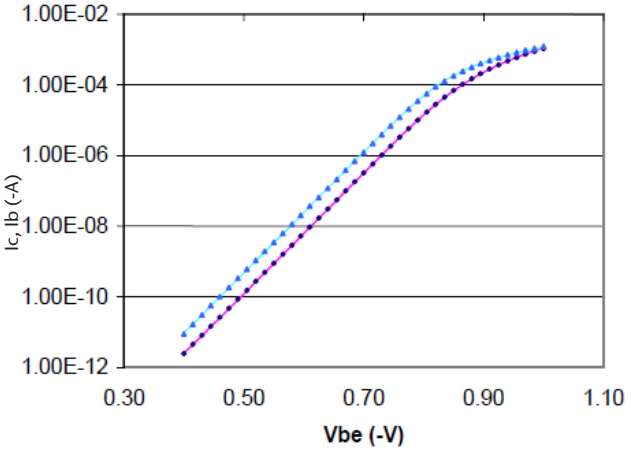
XA035 HV CELLS

Device	Library Feature	Voltage Range	ESD Level	Application benefits
HV_CELLS	Special LV I/O, operating voltage specific HV ESD protection cells	LV, 12V-100V	2kV-8kV HBM	MOS Customized I/O Design
HV_CELLS_MID	Special LV I/O, operating voltage specific HV ESD protection cells	LV, 12V-100V	2kV-8kV HBM	MOS + MOS5A Customized I/O Design

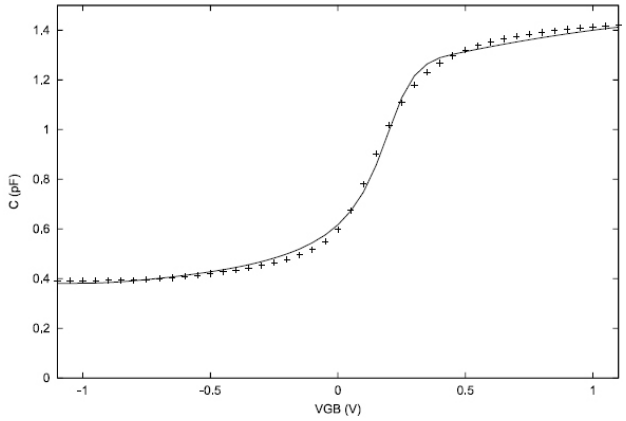
EXAMPLES FOR MEASURED AND MODELED PARAMETER CHARACTERISTICS *



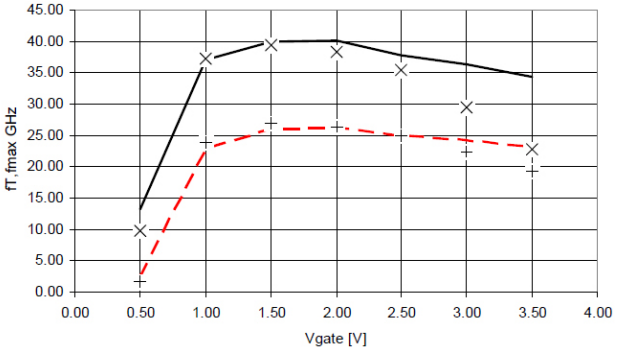
Device nmos: drain current matching vs. Vgs (typical value) legends show the drawn transistor lengths and widths



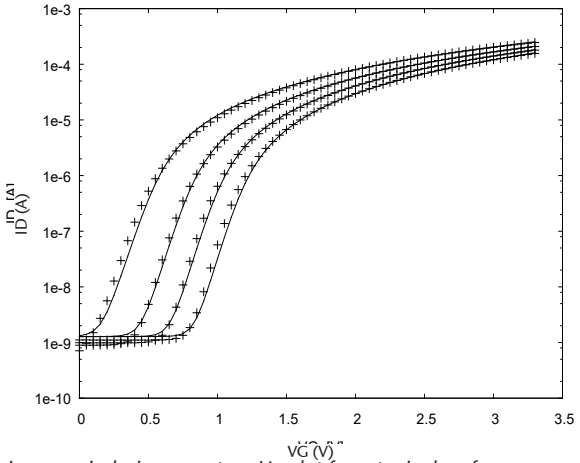
Device qp1: Gummel plot of vertical PNP bipolar transistor 8 µm² Emitter dotted line = measured, solid line = SPICE model



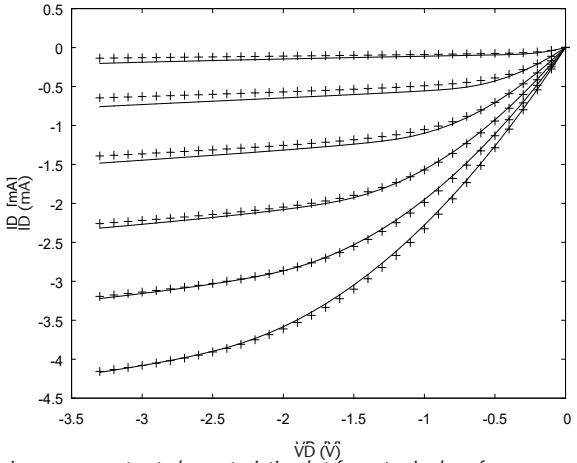
Device mosvc: Capacitance vs. VGB characteristic of MOS varactor for a typical wafer, width = 10µm, no. of rows = 20, no. of columns = 2, + = measured, solid line = SPICE model



Device nmosrf: Ft/Fmax vs. Vg plot, W=10, L=0.35, M=8, Vd=2.5V, +=Ft measured, dashed line=Ft simulated, X=Fmax measured, solid line=fmax simulated



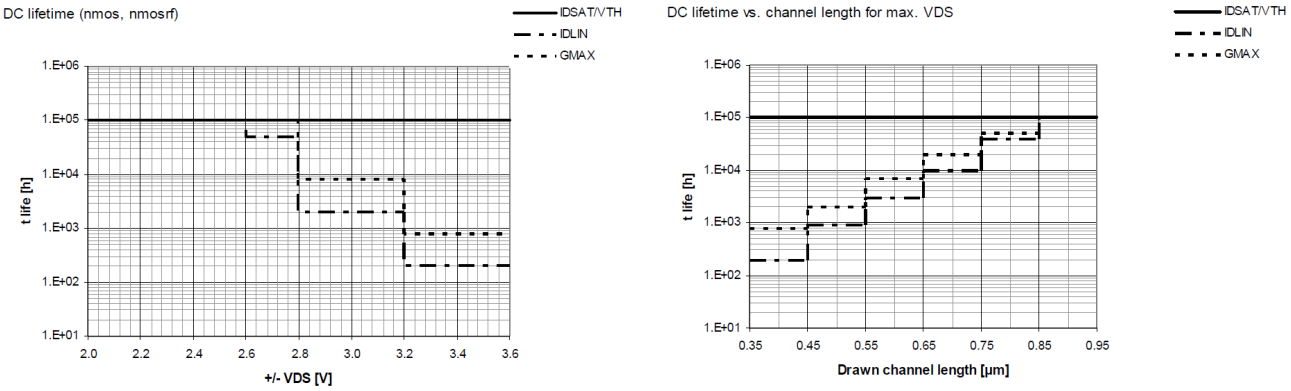
Device nmosi: drain current vs. Vg plot for a typical wafer at 175°C W/L = 20/20, +=measured, dotted line=BSIM3v3, Solid line=BSIM3v3



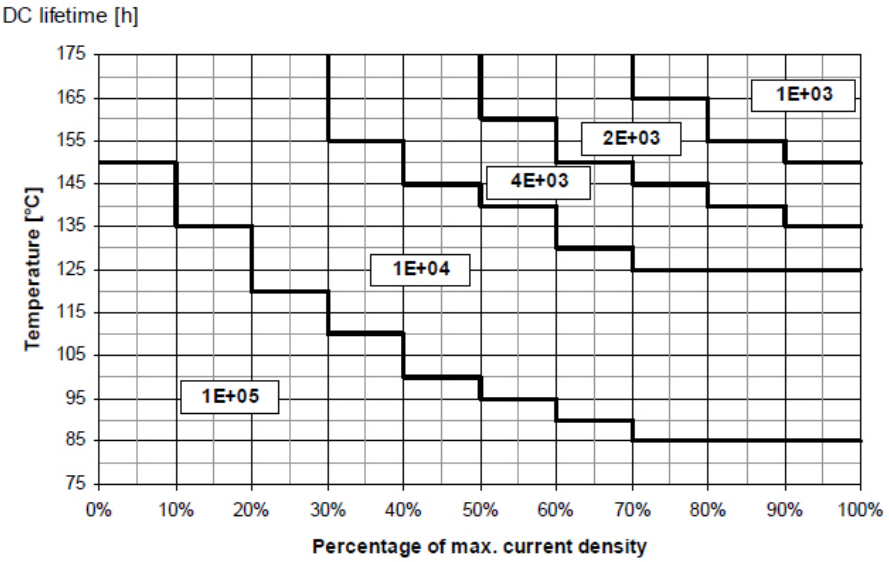
Device pmos: output characteristic plot for a typical wafer at 175°C W/L = 20/0.35, +=measured, dotted line=BSIM3v3, Solid line=BSIM3v3

* The simulation models are valid in the junction temperature range -55 °C ≤ Tj ≤ +185 °C

EXAMPLES DEVICE & LAYER RELIABILITY WITHIN THE MAX. OPERATING CONDITIONS (P.R. PLOT)

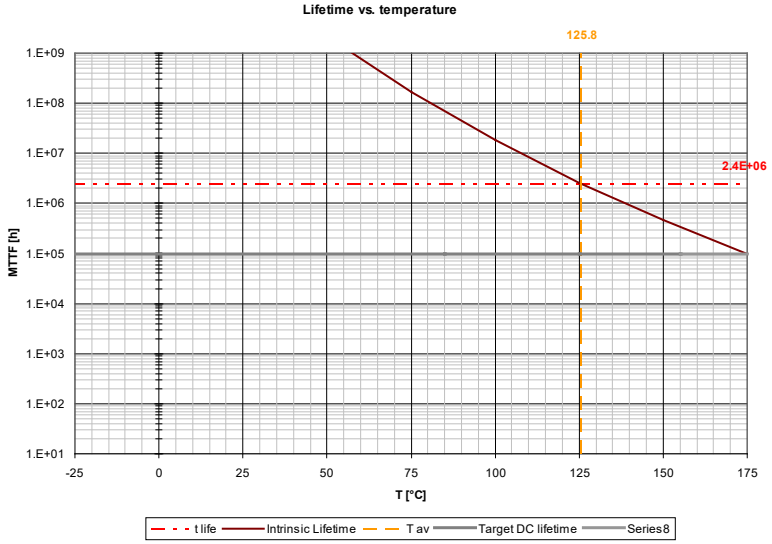


Device nmos, nmosrf: Hot Carrier Injection plots



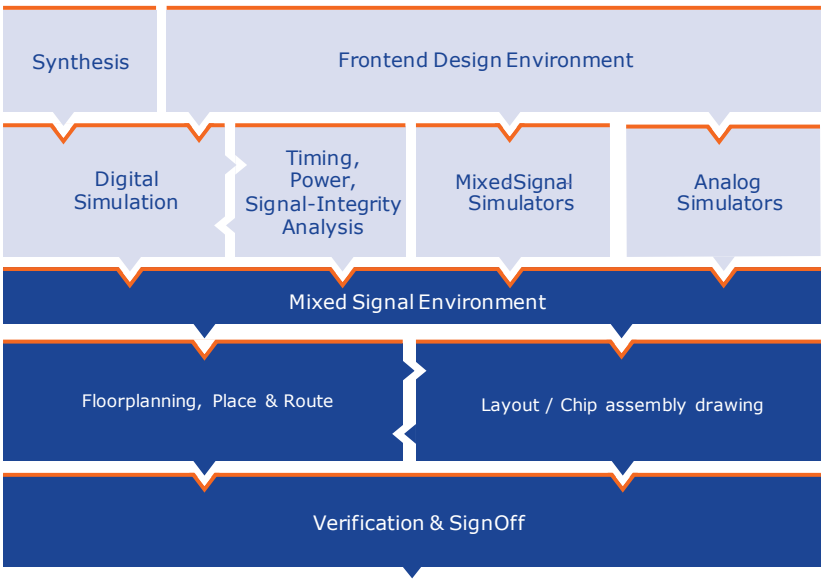
Interconnects Electro Migration / Stress Migration plots

EXAMPLES OF SIMULATED RESULT FROM LIFETIME CALCULATOR TOOL



Example of lifetime vs. temperature plot from the Liftime Calculator Tool for 3.3V Pmos device

XA035 SUPPORTED EDA TOOLS



Note: Diagram shows overview of reference flow at X-FAB. Detailed information of suported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center X-TIC.

X-FAB'S IC DEVELOPMENT KIT "THEKIT"

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