Cyclic RSD ADC in SOI for sensor readout

Introduction

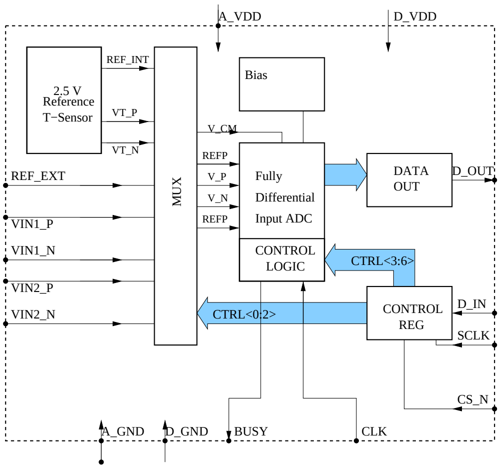

Figure 1: Blockdiagram of the sensor readout

One of the main tasks of IMMS in last years was research and development of cyclic ADC's based on RSD algorithm usable as core for embedded applications. The special advantage of this type of ADC is the reduced complexity of hardware resp. layout area because of the reuse of the main stages for each bit.

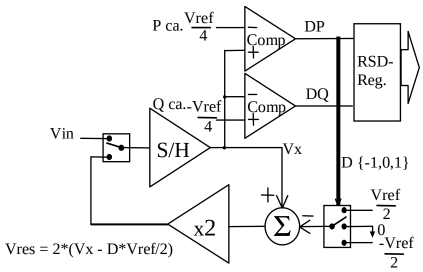

Figure 2: Basic blockdiagram of a cyclic RSD ADC

Up to 13 bit of resolution and linearity are possible without special digital calibration techniques but by use of some special analogue techniques, based on fully differential switched capacitor (SC) techniques. Some special SC system concepts were developed and evaluated by prototypes using different technologies of X-FAB foundry. The main characteristics to distinguish such concepts are given by categories as:

- Capacitor ratio sensitive or insensitive system
- Usage of correlated sampling techniques for correction of offset and/or finite gain of opamps

Use of such techniques increase the effort of hardware (switches, capacitors and opamps) and/or conversion time (needed switching phases per bit).

The ADC realised in a high temperature SOI sensor readout abdicates to such techniques. This implies the need of high capacitor matching and high gain OpAmps but leads to a very simple concept that needs only one fully differential OpAmp and provides one bit in each SC-phase. This concept is a good base for applications with moderate sampling rates where larger capacitors are possible. The complete Chip provides a 2 Channel 12Bit ADC with on chip Temperature Sensor realized in XI10 technologie of X-FAB foundry.

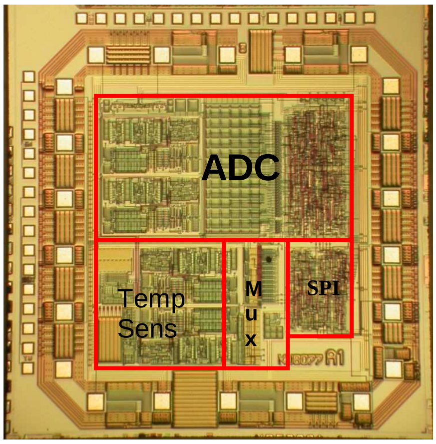

Figure 3: Die photo of the sensor readout

Description of the ADC

For design a high gain single ended precision OpAmp was developed which is used in the ADC as well in the temperature sensor. That's why the fully differential (FD) principle of the ADC concept was modified to a pseudo fully differential (PFD) system replacing the FD OpAmp by two single ended OpAmps. Special techniques were developed to solve some common mode problems which differ from that in a real FD technique; particularly the PFD –Technique has a fixed middle Voltage (VCM) for both OpAmps but nevertheless a common mode error caused by OpAmp offsets can shift the cycling common mode voltage to the rails. The resistive loadable outputs of the used OpAmp enable an easy way for solving this problem.

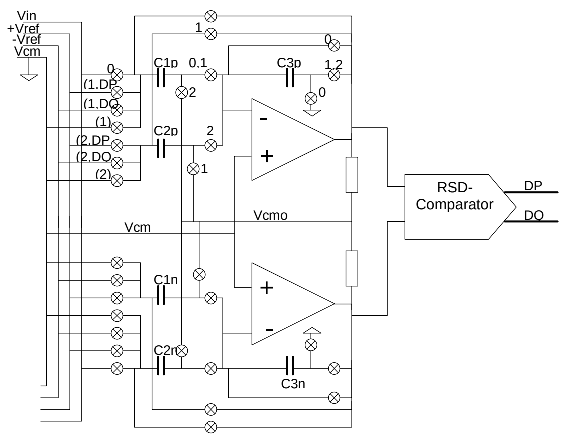

Figure 4: Simplified SC-Concept of the realized cyclic ADC in Pseudo Fully Differential Technique

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Another special technique is implemented to reduce the effect of a difference between the common mode voltage of the input source and VCM of the ADC.
The ADC provides a 16 bit signed integer digital output. The resolution is adjustable from 13 to 16 bit. In practice the 13 bit mode (12 bit resolution + sign) is enough to exploit the reached INL of 12 bit ±0.5 LSB.
In the complete chip the ADC is supported by a serial SPI-Interface, but for use as separate core the direct interface with parallel port is given in Fig. 5.
It has 3 calibration modes adjusted by Inputs KP,KN for measuring the codes for Vin=0 (Offset) ,Vin=Vref, Vin=-Vref (Fullscale).

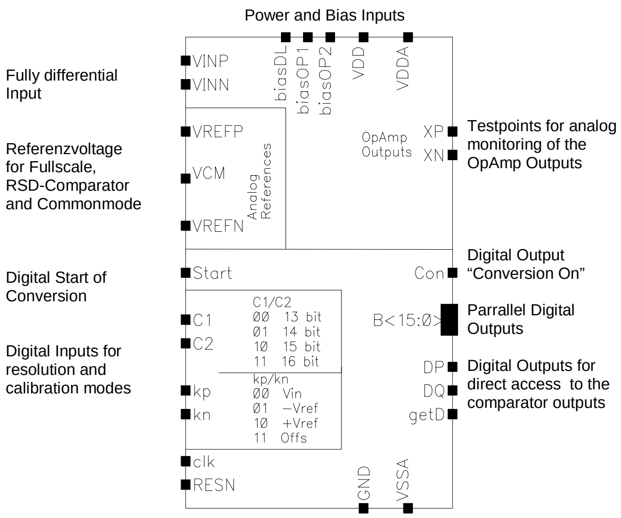


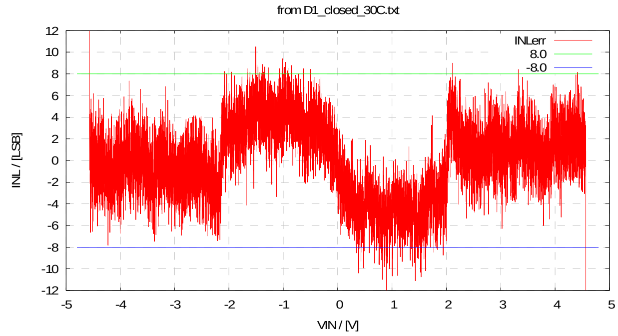
Figure 5: Interface of the ADC-Core

The complete chip has an internal resistive voltage divider for providing the reference voltages for the internal inputs (VREFP,VREFN,VCM). This can be also included when using only the ADC as core. Otherwise the user may provide his own direct sources depending from the application. Also the on chip bias source may be reused or provided by user.

Results

The first prototype works up to 200°C safely at a samplerate of 10 kS/s with a linearity that matches a 12 bit ADC.
The table gives an overview on main characteristic parameters. Fig. 6 shows typical INL-Curves for the full resolution of 16 bit at a clock rate of 50 kHz at temperatures of 30°C and 180°C from the same chip. It shows that the systematic linearity error is decreasing somewhat at higher temperatures.

30°C :



200°C

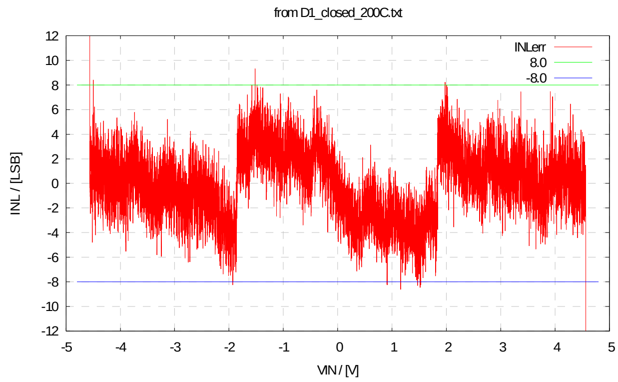


Figure 6: Typical Integral Nonlinearity at Resolution of 16 Bit

parameter	explanations	values
Resolution (resol)	Adjustable by C1,C2	13 ..16 Bit (or 12..15 Bit + Sign)
Linearityerror (INL)	for 13 bit resolution for 16 bit resolution	+/- 1 LSB +/- 8 LSB
Max. Offset	for 13 bit resolution for 16 bit resolution	+/-0.5 LSB +/- 5 LSB
ENOB	(Effective number of bits)	11.6 … 12 Bit
Temperature range	tested range: 20 °… 230°	-50 ℃ … 200℃
maximum clock rate	fclk (at clk input) recommended 100 kHz	200 kHz
Sampling rate	= fclk/(1+resol)	max. 14 kS/s (guarantied 6 kS/s)
max external reference voltage (Vref_ext)	between VREFP,VREFN of Chip	5V (0.8*VDDA)
Fullscale Voltage (Vref)	by resistive on chip voltage devider = 0.92 * Vref	4.6V at Vref_ext=5V (VDDA = 5.5 V)
Layout area of ADCcore	without Biassource and Vref/Vcm-voltage pre divider	920u x 1620u
Quiescent current consumption	For complete sensor chip with 4 OpAmp's	Analog Part: max 2 mA Digital Part: max 25uA

Table 1: Main Parameters

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