

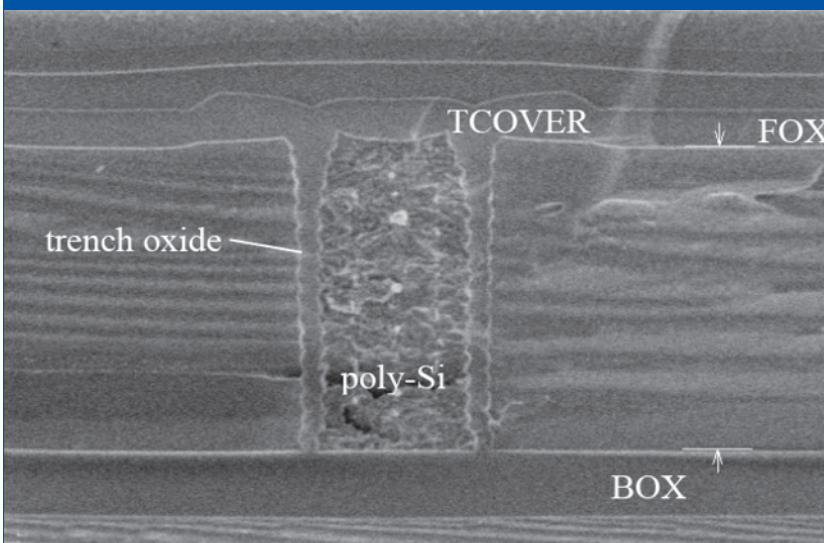
> XT06

SOI CMOS with extended HV Technology

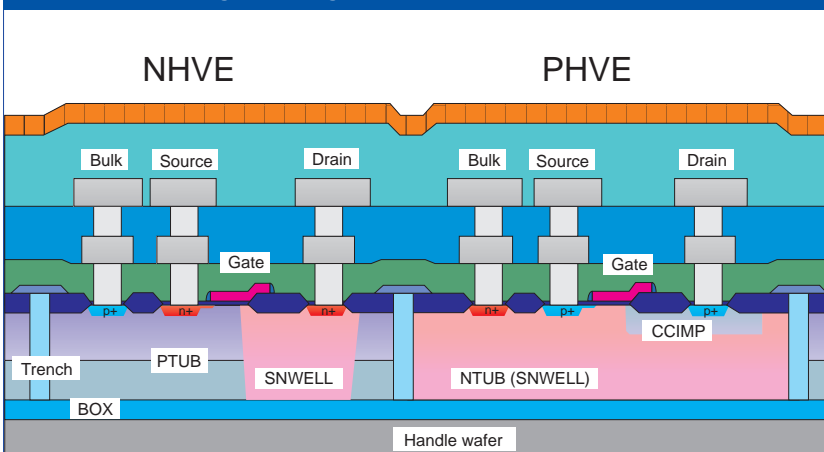
> Modular 0.6 μm Trench Isolated SOI CMOS process for analog/mixed-signal and high-voltage applications.

The process offers reduced parasitics which results in smaller crosstalk, reduced noise and better EMC characteristics.

> XT06 Trench Isolation Cross Section



> Extended High-voltage Device



> Module Overview

CORE

CORE

5V MOS, 1P2M, 6" p-type SOI, trench isolation

FEOL

MIDOX

Mid-oxide module for MV/HV elements

PMV

Medium-voltage P-channel module

NGD

Extended MV n-channel module

DEPL

MV/HV depletion NMOS module

HVS

HV 40V PMOS, ext. HV 60V NMOS module

HVE

Ext. HV 20V NPN, 60V m-DMOS module

PHVE

Extended HV 60V PMOS module

CAPRES

Duble poly capacitor/resistor module

LINC

Linear capacitor module

SCHOTTKY

Schottky diode module

ESD

ESD implant module

HWCONT

Handle wafer contact module

BEOL

METAL3

Triple metal module

THKMET

Thick third metal module

OPTO

Optical window module

PIMIDE

Polyimide module resilient barrier

LIGHTSLD

Light shield module

0.6 μm CMOS Process Family

> XT06

Features

- XT06 unique devices:
 - forward diodes
 - unrestricted 60V high and low side operation of all devices
 - reduced parasitics and crosstalk, better EMC
- Option of arraying HV NMOS devices
- Handle Wafer Contact module, Light Shield module
- High precision BSIM3V3 SPICE models for CMOS and Gummel Poon model for bipolars
- Excellent analog performance with accurate device matching
- Different digital core cell libraries optimized for speed, low power, low noise or, inherited power connection concept
- High density RAM, DPRAM and ROM blocks
- Optional ESD module for higher ESD protection
- OPTO module with optical window for improved transparency
- OTP option (poly fuse or Zener Zap)

Design Rules		
Parameter	Width [μm]	Spacing [μm]
Trench	2	6
N-well	4	2
HV N-well/ P-well	6	3 / 8.5
Active Area	0.6	1.2
Polysilicon Gate	0.6	0.8
Contact	0.6	0.6
Metal 1/ 2	0.9	0.8
Via 1/ 2	0.7	0.6
Metal 3	1.2	1.0
Via/ Met L	0.7 / 2.5	0.7 / 2.5

Capacitors (Selection)			
Parameter	Area Cap [fF/μm ²]	BV [V]	Max VCC [V]
poly0/poly1 cap.	1.87	30	8
linear poly0/poly1 cap.	1.02	20	8
poly1/M1/M2 cap.	0.010	-	60
SNWELL/poly1/M1/M2 cap.	0.13	-	60



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MOS Transistors (Selection)				
Parameter	VT [V]	RDson [kΩ.μm]	BVDSS [V]	Max VDS [V]
bulk isolated PMOS 5V	0.94	-	12	5.5
NMOS with ESD implant	0.90	-	11.5	5.5
NMOS MV low doped drain	0.88	4.5	22	12
NMOS MV low doped s/d	0.88	5.3	22	12
MV depletion NMOS	1.1	-	16	8
PMOS MV low doped drain	0.90	20	18	12
PMOS MV low doped s/d	0.90	26	18	12
bulk isolated MV PMOS	1.25	17	13	8
NMOS HV	0.82	30	60	30
NMOS HV depletion	1.25	16	60	30
PMOS HV	0.82	39	70	37
NMOS extended HV	0.72	23	80	60
PMOS extended HV	0.78	50	80	57
extended HV NDMOS	1.10	28	110	60

Bipolar Transistors (Selection)			
Parameter	BETA	VA [V]	Max VCE [V]
Vertical PNP	15	> 100	5.5
Vertical NPN	60	> 100	20

Forward Diodes (Selection)			
Parameter	Vf [V]	Max If [mA/μm]	Max Vr [V]
rectifier diode (dfwdn)	0.76	0.3	10
rectifier HV diode (dfwdph)	0.76	0.3	50

Schottky Diode			
Parameter	Vf [V]	If [μA]	BV [V]
scalable Schottky diode	0.34	100	21

Resistors (Selection)			
Parameter	RS [Ω/□]	VA [V]	Max VCE [V]
low TC poly0 resistor	580	-0.20 / 0.80 *	60
high resistive poly0 resistor	3500	-3.3 / 10.9 *	60

* linear / quadratic temperature coefficient

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