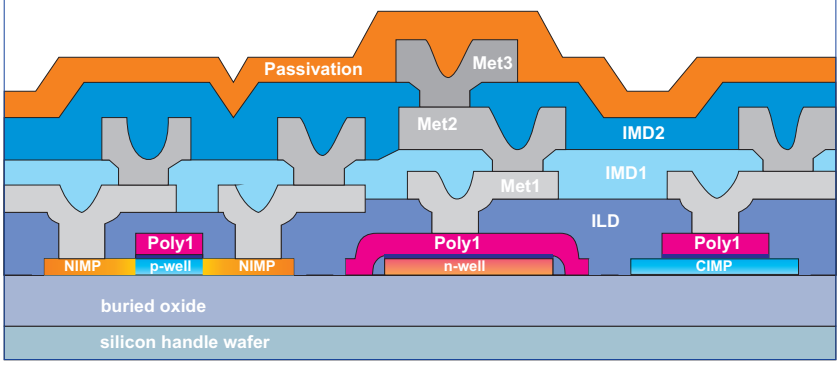
1.0 µm SOI Process

1.0 µm Silicon-On-Insulator Technology

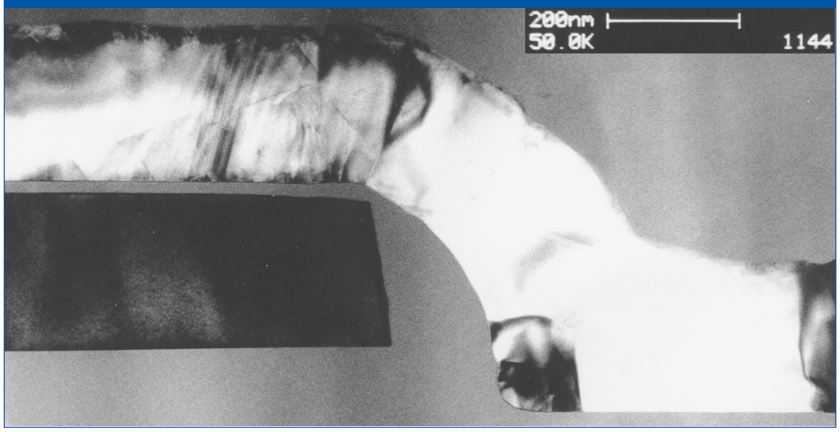
1.0 µm Non-fully Depleted SOI Technology with:

- 1000 nm Box Oxide
- 250 nm Active Silicon
- 25 nm Gate Oxide Thickness

1.0 µm transistor cross section



Cross section through transistor



Applications

- Dielectric Isolated Mixed-Signal (multi voltage systems)
- High Temperature
- High Voltage
- Intrinsic Radiation Hardness
- 42 V Automotive Board Net

Features

- fully dielectric isolated twin well 3 metal layers with high temperature option up to 225°C operating temperature
- 5V N-and P- MOS transistors in SOI specific layout variants
- DMOS high voltage capability up to 130V breakdown voltage
- hall sensor
- 13 mask layers, 14 mask layers with linear capacitor option

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Process Features & Typical Electrical Parameters

Analog

- BSIM3SOI (b3soipd) transistor models
- Fully isolated diodes
- Different types of passive devices
- Hall plate for magnetic field detection
- Analog cell library in development

Digital

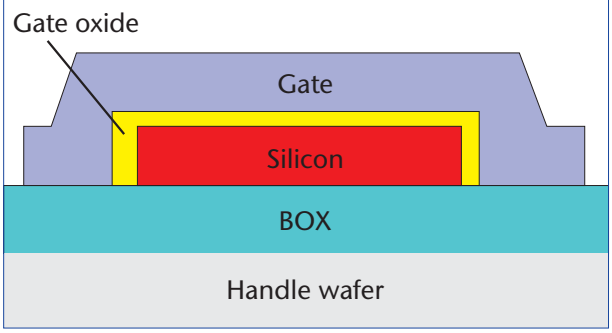
- Low power high temperature digital core library
- SRAM memory blocks in development
- I/O Library in development

Optional Analog Capabilities

- Linear capacitor
- High resistive poly resistor

Design Rules	
Element	Pitch [µm]
Gate	2.2
Metal 1	2.3
Metal 2	2.3
Metal 3	4.0
Trench	2.4
Contact	1.9
Via 1	2.4
Via 2	2.4
Enclosure:	
Contact - Metal 1	0.5
Metal 1 - Via	0.5
Via - Metal 2	0.5
Metal 2 - Via 2	0.5
Via 2 - Metal 3	0.6

Principle of SOI transistor



Analog Elements	
POLY-TRENCH capacitor:	
Capacitance	0.99 fF/µm²
Equivalent oxide thickness	35 nm
Linearity	< 500 ppm/V
High Resistive Poly Resistor - HiRes:	
Resistance	1.3 kΩ/☐

High Voltage Elements			
Parameter	Unit	n-channel	p-channel
VT	V	1.65	- 1.10
BVMAX 3µm	V	70	- 60
BVMAX 6µm	V	100	tbd
BVMAX 10µm	V	130	tbd

Sheet Resistances	
Material	[Ω/☐]
RDIFFN	45
RDIFFP	65
RPOLY	30

Typical 5V SOI-CMOS Parameters			
Parameter L=1µm body tied	Unit	n-channel	p-channel
VT	V	1.65	- 1.25
IDS 6x1H	µA	900	- 600
BVDSS	V	12.5	- 12.5

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