



## Operation principle

The I<sup>2</sup>C Bus is inactive when both lines lead HIGH level . The start of a data transmission is introduced by the creation of a start condition by a participant willing to send. The data transmission takes place in blocks of 8 bit each and an acknowledge bit. With the acknowledge bit the sending participant is informed of the correct data reception by the addressed receiver. With the creation of the stop condition the data transmission is stopped

The selection of the reception node intended to be addressed takes place over an individual 7 bit wide address. It is transmitted as first data byte in the I<sup>2</sup>C protocol to all bus participants In this case the addressed bus node is acknowledging his prime to receive in the acknowledge bit.. If there is no addressed bus participant, the sender has to stop the transmission by sending a stop bit.

In the I<sup>2</sup>C bus protocol a participant arbitration for the multimaster mode is implemented. In this way it is ensured that- if there is a simultaneous will to send of several bus nodes- the bus node with the least significant participant address is successful as sender of data.

Over the address 00h (General Call) an initialisation information can be transmitted to all bus nodes.

## Characteristics

The connection of the macro cell to the I<sup>2</sup>C bus takes place over a Open-Collector I/O level. However, an external device is not necessary (bus driver etc.).

The start of a data transmission is introduced by activating of the line *st\_tr*. If the I<sup>2</sup>C bus is inactive, the data byte contiguous to *sr\_data\_i* is transmitted on the I<sup>2</sup>C bus. If the addressed data node is acknowledged correctly, then the data byte that is to be transmitted next is demanded over *ack*. After connecting to *sr\_data\_i* it has to be acknowledged by activating *qack* . If the acknowledge bit is missing, the controller stops the data transmission.

If the controller is receiving his node address on the I<sup>2</sup>C bus, then this process of the circumference is indicated by activating *aas*. After reception of the first data byte *ack* is activated . The circumference is acknowledging the correct reading of the data bytes by *qack* and the controller is signalling the readiness for reception of further data. If *qack* is not activated, then the acknowledgement of the receiver node is missing and the transmitting node stops the transmission of further data bytes.

The entries and exits of the macro cell have been described completely and unidirectional in order to facilitate the implementation in a larger integrated circuit for a posterior use. However, for the 8 bit data bus a control pin exists in order to complete this pin into a bi-directional data bus. The bus participant address and the division factor for the data transmission rate are to be turned on durably at the entries. The data transmission rate is determined as following:

$$f_{SCL} = \frac{f_{clk}}{8(cldata + 1)}$$

In this way the data transmission rate on the I<sup>2</sup>C Bus can be adapted to individual needs.

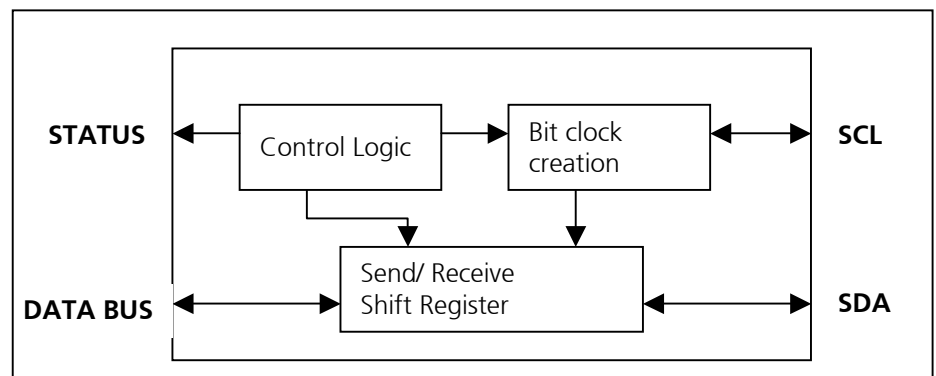


Fig. 3: Block Diagramm