

8-bit Controller-Core IPMS_16CXX

Features

The controllercore IPMS_16CXX realizes a to the PIC 16CXX-family of the firm Microchip compatible 8-bit microcontroller.

An efficient command, the extensive periphery and multitude existing software solutions are some of the most striking features of this controller. Our microcontrollercore is structured at the Harvard architecture. This architecture makes possible a parallel access on program and data memory.

The microcontrollers RICS-command includes 33 orders. All orders with the exception of the branch operations are processed in an only transfer command.

The instruction process results with a two-phases pipeline. Thereby an efficient processing of all orders is reached including the branch instructions.

In the first phase the shop of the instruction results from the program memory. In the second phase the instruction will decode and execute.

The controllercores clock scheme agrees with the model. It is with it possible, already existing PIC-software solutions take over on the IPMS_16CXX-controllercore without changes.

Storage capacity and controller periphery can be adjusted individual demands. An expansion of the controllercore through additional periphery devices is possibly. The synthesizability of the controller description allows a simple taking over of the microcontrollers on other ASIC-technologies.

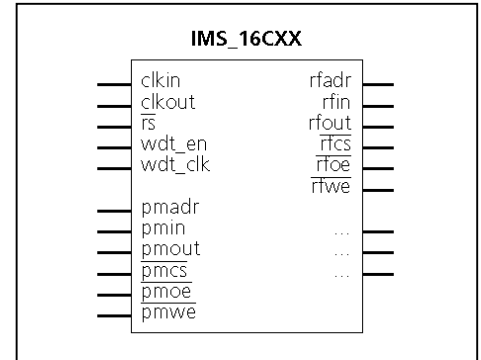


Fig. 1: 8-Bit Controller Core

An implementation of the controller description in a XILINX-FPGA is tested likewise possible and became already.

The following index (Fig. 2) shows the I/O-pins basic configuration.

pin name	I/O	function
\overline{rs}	I	system reset
clk _{in}	I	input clock
clk _{out}	O	system clock
wdt _{en}	I	watch dogenable
wdt _{clk}	I	watch dogtimer clock
\overline{Pmadr}	O	program memory control
\overline{Pmcs}	O	
\overline{Pmoe}	O	
pmin	I	
\overline{rfadr}	O	data memory control
\overline{rfcs}	O	
$\overline{rf\oe}$	O	
rfwe	O	
rfin	I	
rfout	I	

Fig. 2: Configuration of the I/O-Pins

The amount further pins are determined by the periphery devices application.

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The memory devices control results like in fig. 3 presented clock scheme.

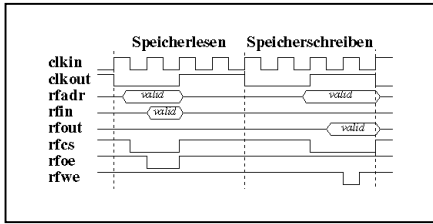


Fig. 3: Clock scheme to control the memory devices

The schematic diagram (fig. 4) shows beside the controller architecture available periphery devices, which can include application specific elements of the controllercore.

Application

- controllercore area without periphery devices in Nand2-equivalents: 1151
- microcontroller or substitute the control unit in ASIC-applications
- ASIC with memory configuration for microcontroller applications
- controller realization in FPGA-applications

Specification

- hardware realization of a 8-bit microcontroller, compatible in command, architecture and clock rate to the PIC16CXX-family
- synthesizable VHDL-model in IEEE-standard 1076-1987 for use as macrocell in ASIC's
- 8-bit arithmetic (addition, subtraction, logical operations, bit manipulation)
- to 64 k instruction words program memory
- to 512 bytes data memory
- maskable interrupt system
- power down mode
- optional periphery like ports, timer and interfaces according to model

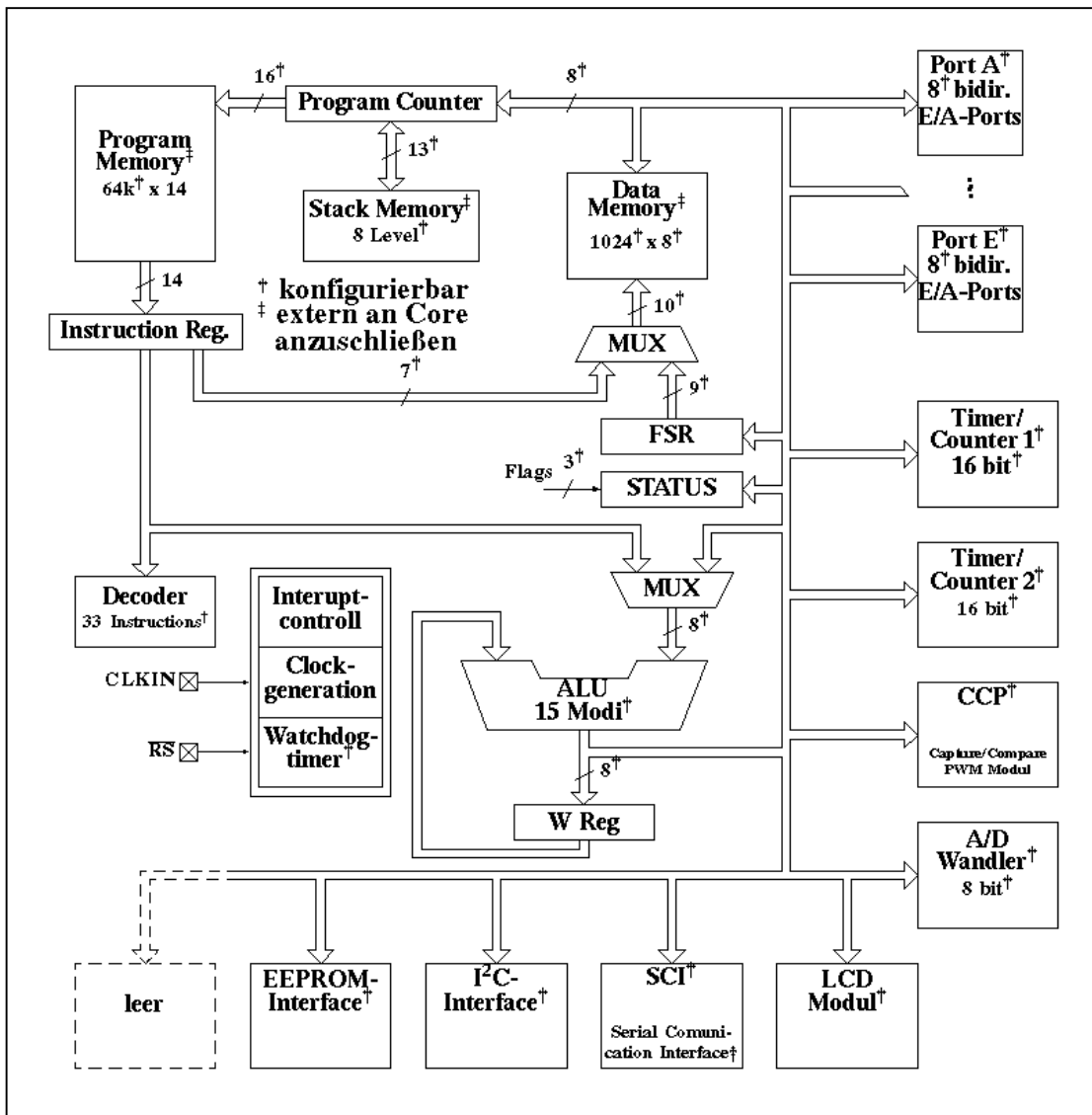


Fig. 4: Schematic diagram of the controllercore