

Description

The IPMS_16550 (fig. 3) has separate transmitter and receiver modules. Each of them can use a 16 byte FIFO memory.

Transmitter and receiver can work with different data ratings. The rating for the transmitter is the result of a programmable divider.

An oscillator frequency of 1,8432 MHz for example allows ratings from 50 to 115200 baud.

The resulting main frequency is available at the output TxCLK. The frequency for the receiver is RxCLK. When the input RxCLK is shorted to TxCLK, receiver and transmitter are working with the same rating.

The receiver control logic detects framing, parity and data bits. The receiver register is double buffered or with 16 byte FIFO buffered.

The transmitter adds framing and parity information to the data. The transmitter register is also double buffered or with 16 byte FIFO buffered.

The modem control logic realize signals like RS232C.

Programming and data transfer from the host side is implemented by an 8 bit wide databus. The data rating, the count of databits and stopbits, also the parity information and FIFO's, are programmable with these registers.

Software compatibility to the UART 16550 make it easy to implement them in their own systems.

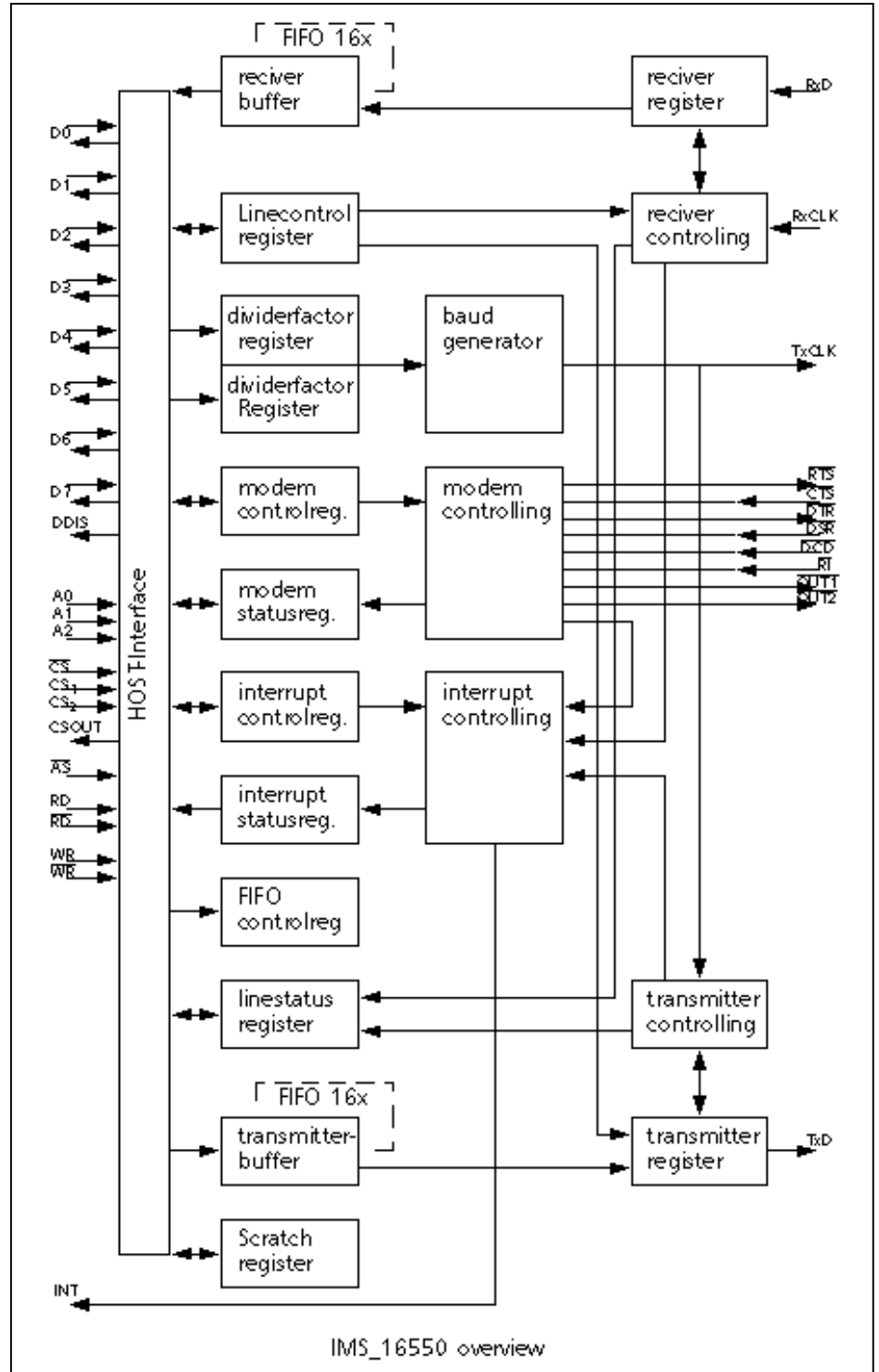


Fig. 3: Block diagram of the IPMS_16550