

> XP018

Modular CMOS Power Management Process Technology

> XP018 is X-FAB's specialized process for power management applications.

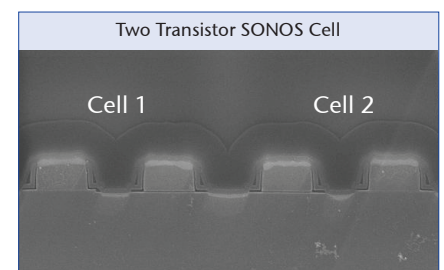
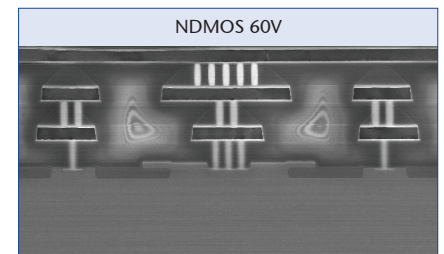
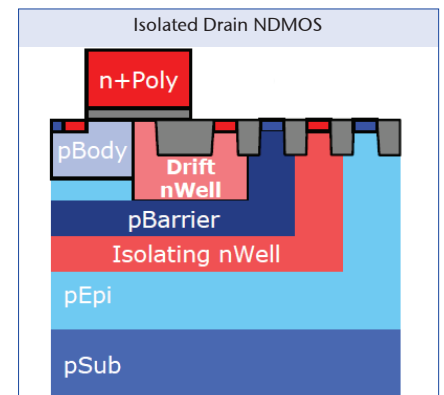
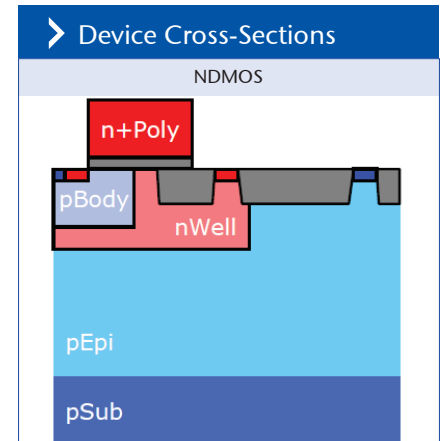
It is especially suited for applications needing an integrated solution and cost efficient process for power management ICs. Targeted applications are switching applications, lightings, display, etc, operating in temperature range of -40 to $+125^\circ\text{C}$.

> Module Overview

CORE	Remarks
LP5MOS 1.8V/5.0V 1P4M low power MOS module	23 masks (masks equals process layers unless noted otherwise)

FEOL	Remarks
ISOMOS Isolated CMOS module	+1 mask is prerequisite for NVM, DMOS1, DMOS2, HV MOS
DEPL Depletion module	+1 mask
NVM Non-volatile-memory module	+5 masks (+4 only if HV modules/ ISOMOS is selected) MIM (+1 mask) may be needed for charge pump
HVA High voltage module	+2 masks (+1 only if ISOMOS is selected) nDMOS, pDMOS, HV PMOS, NPN bipolar transistor
HVB High voltage module	+1 masks HV NMOS
HVC High voltage module	+4 masks (+3 only if ISOMOS is selected) isolated drain nDMOS and NPN bipolar transistors
HVD High voltage module	+3 masks (+2 only if ISOMOS is selected) HV PNP bipolar transistor

BEOL	Remarks
MIM MIM capacitor module	+1 mask
DMIM Double MIM capacitor module	+1 layer
TMIM Triple MIM capacitor module	+1 layer
5METALS 5 metal layers module	+2 masks
6METALS 6 metal layers module	+2 masks
THKMET Thick metal module	+2 masks
PIMIDE Polyimide module	+1 mask



0.18 μm CMOS Process Family

> XP018

Features

- 1.8V logic layout & performance compatible with industry standard, 5V dual gate process
- Integrated digital, analog, HV and NVM in a single process
- High-reliability NVM using SONOS technology
- Very low mask count for an integrated analog process with HV and NVM
- 15V ~ 60V DMOS with high-side capability
- Isolated drain NDMOS
- High density up to 125000 gates per mm²
- I/O cell library with 4kV HBM ESD protection levels
- Typical and worst-case models - BSIM3v3.24 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterised & included in model
- Diva, Dracula, Assura, Calibre, Hercules DRC & LVS parasitic extraction

Bipolar Transistors (Selection)

Parameter	BETA	VA [V]	VBE [mV]	Max VCE [V]
Vertical NPN (qnva)	55	15	695	3.6
Vertical NPN (qnvb)	105	25	605	10
High Voltage PNP	100	170	610	60

Schottky Diode

Parameter	Forward Voltage [V]	BV [V]
dsa (LP5MOS)	0.38	8.5
dsb (ISOMOS)	0.45	18

Non-Volatile Memory

Parameter	Memory size [bit]	Data retention	Configurations bits x words
eFlash	1M	10yrs @125°C	32 x 32k
EEPROM	1k...128k	10yrs @125°C	8x128...32x16k
OTP	1k...128k	10yrs @85°C	8x128...32x16k

Design Rules

Parameter	Size [μm]
N-well width	0.86
Active Area width	0.22
Polysilicon Gate	0.18
Contact / Metal 1 width	0.22 / 0.23
Via / Metal width	0.26 / 0.28
Top Via / Metal	0.36 / 0.44

MOS Transistors (Selection)

Parameter	VT [V]	IDS [μA/μm]	BVDSS [V]	Max VDS [V]
1.8V NMOS	0.60	480	> 3.6	1.8
1.8V PMOS	0.65	170	> 3.6	1.8
5.0V NMOS	0.78	550	> 8.0	5.5
5.0V PMOS	0.86	250	> 7.5	5.5
Isolated 5.0V Depl. NMOS	0.52	730	> 8	5.5
15V PMOS (symm.)	0.89	40	> 25	15
30V NMOS (symm.)	0.85	110	> 40	30
45V PMOS (symm.)	0.89	18	> 55	40/45*

DMOS Transistors

Parameter	VT [V]	BV [V]	RON.A [mΩ.mm ²]	Max VDS [V]
15V NDMOS	0.88	> 19	21	15
15V PDMOS	0.88	> 24	53	15
25V NDMOS	0.88	> 28	39	23/25*
25V PDMOS	0.92	> 35	100	25
40V NDMOS	0.88	> 43	75	35/40*
40V PDMOS	0.92	> 45	165	35/40*
60V NDMOS	0.88	> 62	110	50/60*
60V PDMOS	0.92	> 61	255	50/60*
Isolated drain 18V nLDMOS	0.91	> 37	23	13

* Tj = -40°C...+125°C / 0°C...+125°C.

RON @ VGS = 5V

tbd = To Be Determined



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