

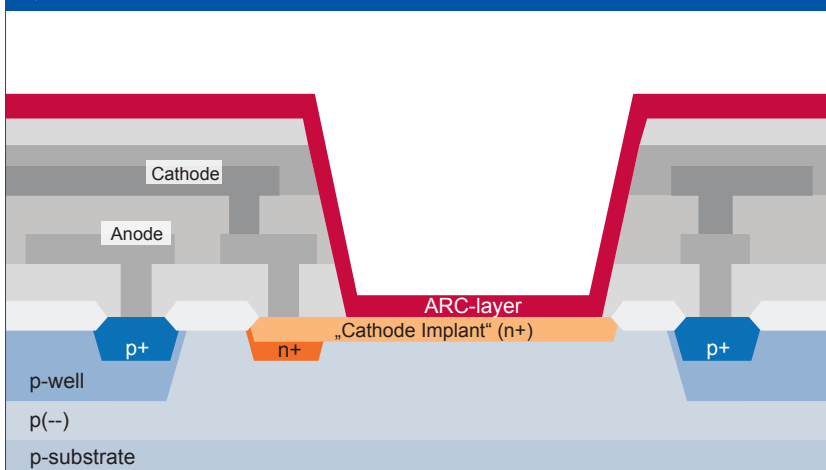
> XO035

Modular CMOS Technology For Fast Optical Applications

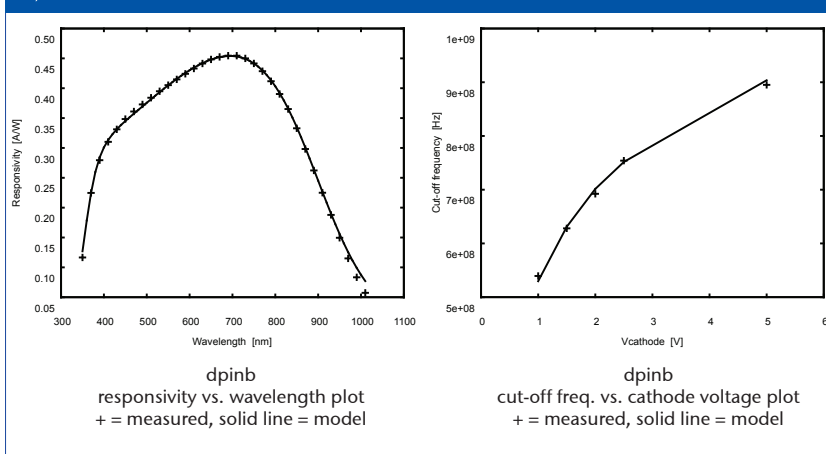
> XO035 is X-FAB's specialized process for optoelectronic and high speed RF applications.

It is especially suited for applications needing sensitive high bandwidth photo diodes arrays or CMOS image sensors for such applications as optical data storage, optical data communication or high dynamic range cameras.

> XO035 PIN diode Cross Section



> PIN diode Characterization



> Module Overview

CORE

MOS

3.3V MOS module, 1P3M

FEOL

MOSSA

Mid gate oxide module

ISOMOS

Isolated MOS module

CAPPOLY

Polysilicon 2 module

HRPOLY

High resistance polysilicon module

PINBLUE

PIN diode module

BEOL

MIM

MIM capacitor module

DMIM

Double MIM capacitor module

OPTO

Optical window module (blue light)

OPTO_RED

Optical window module (red light)

OPTO_IR

Optical window module (infrared light)

METAL4

Metal 4 module

0.35 μm CMOS Process Family

> XO035

Features

- High bandwidth, high sensitivity PIN diode
- Optimized anti-reflective coating (ARC) for blue, red and infrared wavelengths respectively
- Optical window etching supporting 4-metal stacks
- 3.3V logic layout & performance compatible with industry standard, 5V dual gate module
- MIM capacitor for RF and high linear applications
- High density up to 18000 gates per mm²
- I/O cell library with 4kV HBM ESD protection levels
- Typical and worse-case models - BSIM3v3.24 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterised & included in model
- Diva, Dracula, Assura, Calibre, Hercules DRC & LVS parasitic extraction
- Gold and Solder Bump compatible

PIN Diode			
Parameter	Sensitivity [A/W]	cut-off freq. [MHz]	BV [V]
Blue PIN	0.30 @405nm	750 @405nm	> 50
Red PIN	0.52 @650nm	720 @650nm	> 50
Infrared PIN	0.40 @850nm	85 @844nm	> 50

Bipolar Transistors				
Parameter	BETA	VA [V]	VBE [mV]	Max VCE [V]
Vertical PNP	4.5	190	720	3.6
Lateral PNP	27	4.2	730	3.6
Isolated vertical NPN	35	90	685	5.5
Isolated vertical NPN	55	50	685	5.5

Resistors (Selection)			
Parameter	RS [Ω/□]	Temp. Coeff [10 ⁻³ /K]	Max VTB [V]
Low TC poly2 resistor	200	-0.2	18
N+ high res. poly resistor	1000	-2.8	18
N-well resistor	1160	1.1	18



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Design Rules		
Parameter	Min. Width [μm]	Min. Spacing [μm]
N-well	1.6	7.0
Active Area	0.5	0.6
Polysilicon Gate	0.35	0.45
Contact	0.4	0.4
Metal 1/ Via	0.5	0.45
Metal 2/ 3	0.6	0.5
Top Metal 3/ 4	0.5	0.6
Opto	4.0	3.0

MOS Transistors (Selection)				
Parameter	VT [V]	IDS [μA/μm]	BVDSS [V]	Max VGS [V]
3.3V NMOS	0.61	500	> 5.5	3.6
3.3V PMOS	0.74	250	> 5.5	3.6
5V NMOS	0.91	450	> 7	5.5
5V PMOS	0.86	205	> 7	5.5
Isolated 3.3V NMOS	0.59	500	> 5	3.6
Isolated 3.3V PMOS	0.78	240	> 5	3.6
Isolated 5V NMOS	0.91	465	> 7	5.5
Isolated 5V PMOS	1.01	190	> 7	5.5
12V drain NMOS	0.59	97	> 15	3.6

Capacitors (Selection)			
Parameter	Area Cap [fF/μm ²]	BV [V]	Max VTB [V]
poly1/poly2 cap.	0.85	> 26	18
MIM cap.	1.25	> 20	18

Varactor		
Parameter	Tuning range [%]	Q @ 1GHz
Varactor diode	36	35
MOS Varactor	71	50

Programmable Device (Selection)			
Device	Vreverse [V]	Vreverse (fused) [V]	Max Iread [mA]
Zener Zap	4	0.05	0.05

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