

# 0.35 $\mu\text{m}$ CMOS Process Family



## > XO035

### 0.35 Micron Modular CMOS Technology For Fast Optical Applications

#### > Description

XO035 is X-FAB's specialized process for optoelectronic and high speed RF applications.

It is especially suited for applications needing sensitive high bandwidth photo diodes arrays or CMOS image sensors for such applications as optical data storage, optical data communication or high dynamic range cameras.

In addition to the single poly, four metal 0.35-micron drawn gate length process for digital applications, process modules are available for five volt drain-source and isolated transistors, double-poly and MIM capacitor and high resistance poly resistors. Special opto-process modules allow an optimised PIN cathode implantation, optical window etching and dedicated ARC layer deposition.

Bipolar and MOS Transistors are available. A suite of RF active and passive components are also available. A highly sensitive PIN diode supports wavelengths from 400nm to 900nm. It can be optimized for maximum quantum efficiency of blue, red and infra-red light respectively.

All main modules are comparable in Design Rules and Transistor Performance with other state of the art 0.35  $\mu\text{m}$  CMOS Processes. Comprehensive design rules, accurate SPICE models, analog and digital libraries, IP's and development kits support the process on platforms supplied by the major EDA tool vendors.

#### > Key Features

- high bandwidth, high sensitivity PIN diode
- **NEW:** Optical window etching supporting 4-Metal stack
- **NEW:** Optimized anti-reflective coating (ARC) for blue, red and infra-red wavelengths
- 3.3V logic layout & performance compatible with the industry standard
- 0.35-micron single poly, triple metal, N-well CMOS basic process
- Modular concept
- 5V dual gate module
- MIM & DMIM capacitor for RF and high linear applications
- Double poly capacitor
- High value poly resistor
- Well isolated 3.3V and 5V devices
- Diode and MOS varactors
- 4 metal layers for more complex wiring
- Competitive RF performance
- High Density up to 18000 gates per  $\text{mm}^2$
- I/O cell library with 4kV HBM ESD protection levels
- Typical and worst-case models - BSIM3v3.24 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterised & included in model
- Diva, Dracula, Assura, Calibre, Hercules DRC & LVS & parasitic extraction
- RF characterisation and models for all RF MOS transistors and passive components
- Gold & Solder Bump compatible

#### > Applications

- Mixed signal embedded systems with photo detector
- CMOS Image Sensors with control logic
- High Precision mixed signal circuits
- RF Applications

#### > Quality Assurance

X-FAB spends a lot of effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided

by strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS 16949 and other standards.

#### > Deliverables

- PCM tested wafers
- Optional production services: wafer sort
- Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Service (MLM)
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development

> Digital Libraries	<ul style="list-style-type: none"> <li>- Foundry-specific optimized libraries</li> <li>- Standard core library for high speed digital blocks</li> <li>- Pad-limited IO library</li> <li>- Core-limited IO library</li> <li>- IEEE 1364 Verilog simulation models</li> </ul>	<ul style="list-style-type: none"> <li>- IEEE 1076.4 VHDL-VITAL simulation models</li> <li>- Synthesis libraries</li> <li>- Macrofunction and IP's on request</li> <li>- RAM, DPRAM, ROM</li> </ul>
> Primitives Devices	<ul style="list-style-type: none"> <li>- PIN diode</li> <li>- NMOS/PMOS Transistors</li> <li>- Bipolar transistors</li> <li>- Diodes</li> </ul>	<ul style="list-style-type: none"> <li>- Capacitors</li> <li>- Resistors</li> <li>- Varactors</li> </ul>

> Process Family			
Module Name	No. of Masks	Remarks	Typical Primitive Devices Applications
MOS	14	<b>Standard MOS module</b> Single poly, triple metal CMOS	3.3V NMOS/PMOS and resistors

This main module can be combined with one or more of the following additional modules. Please also refer to the table “**Restrictions for Module Combinations**” because:

- some modules are only available in combination with other modules,
- some modules are not available in combination with other modules.

Module Name	No. of Masks	Remarks	Typical Primitive Devices Applications
MOSSA	3	<b>Mid Gate Oxide module</b>	5V NMOS/PMOS transistors with mid gate oxide (with 3.3V NMOS/PMOS)
ISOMOS	2	<b>Isolated MOS module</b> additional deep N-well and P-well	Isolated 3.3V and 5V NMOS/PMOS
MIM <sup>a)</sup>	1	<b>MIM capacitor module</b> CMM mask for capacitor metal	Capacitors
DMIM <sup>a)</sup>	1	<b>Double MIM capacitor module</b> DMM mask for capacitor metal	Capacitors
CAPPOLY	1	<b>Polysilicon 2 module</b> double polysilicon process	Double poly capacitor, Low TCR poly resistor
HRPOLY	1	<b>High resistance module</b> polysilicon1 module	High value poly resistor
OPTO <sup>a)</sup>	1	<b>Optical window module</b> optimized for blue light	Optical application
OPTO_RED <sup>a)</sup>	1	<b>Optical window module</b> optimized for red light	Optical application
OPTO_IR <sup>a)</sup>	1	<b>Optical window module</b> optimized for infrared light	Optical application
PINBLUE <sup>a)</sup>	1	<b>PIN diode module</b> specific cathode implant, optimized for blue light	PIN diode for optical applications, high efficiency for blue light
METAL4	1	<b>Metal 4 module</b> additional via and metal layer	More complex wiring

Notes: a) For this module, refer to “**Restrictions for Module Combinations**” as listed in the following table.

**Restrictions for Module Combinations**

Module Name	Use of the module also requires use of following modules	Use of the module is not available in combination with the following modules
PINBLUE	OPTO or OPTO_RED or OPTO_IR	
MIM		DMIM
DMIM	METAL4	MIM
OPTO		OPTO_RED, OPTO_IR
OPTO_RED		OPTO, OPTO_IR
OPTO_IR		OPTO, OPTO_RED

> Process Flow

MOS Module	Additional Modules	
Wafer Start		
Active area	DW Implant	ISOMOS
N-well N-Field	PIN Diode Implant	PINBLUE
Poly 1	Dual Gate Oxide High Res. Poly	MOS5A HRPOLY
N- Implant P- Implant	5V N-implant	MOS5A
N+ Implant P+ Implant	Poly 2	CAPPOLY
	NPN Collector	NPN
	NPN Emitter	NPN
	Poly 3	NPN
Silicide Block Contact		
Metal 1 Via 1	DMIM Capacitor	DMIM
Metal 2 Via 2	MIM Capacitor	MIM
Metal 3	DMIM Capacitor	DMIM
	Via 3	METAL4
	Metal 4	METAL4
	Optical Window	OPTO, _RED, _IR
Back side grinding		

mask steps

> Schematic Cross Sections

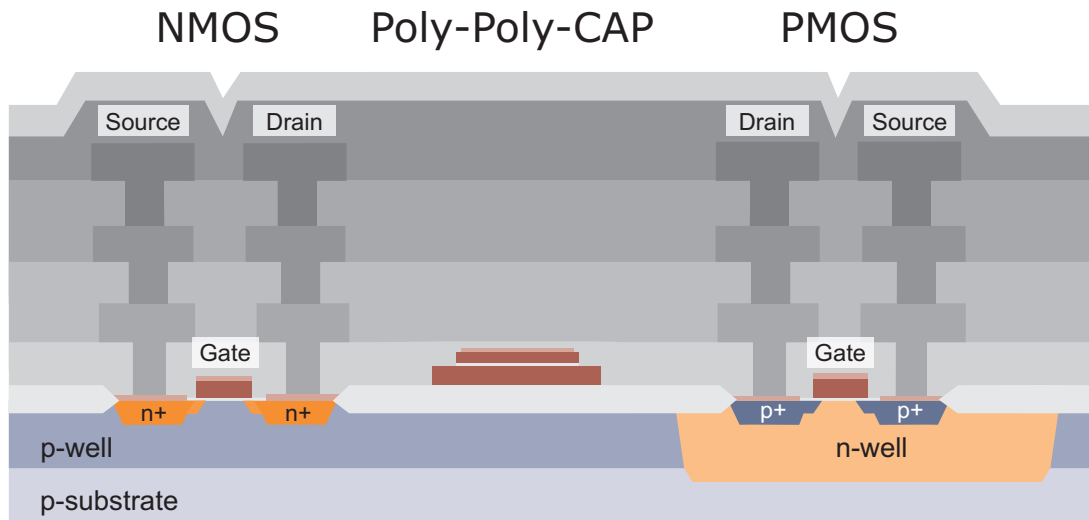


Figure 1: CMOS and Poly-poly capacitor structure

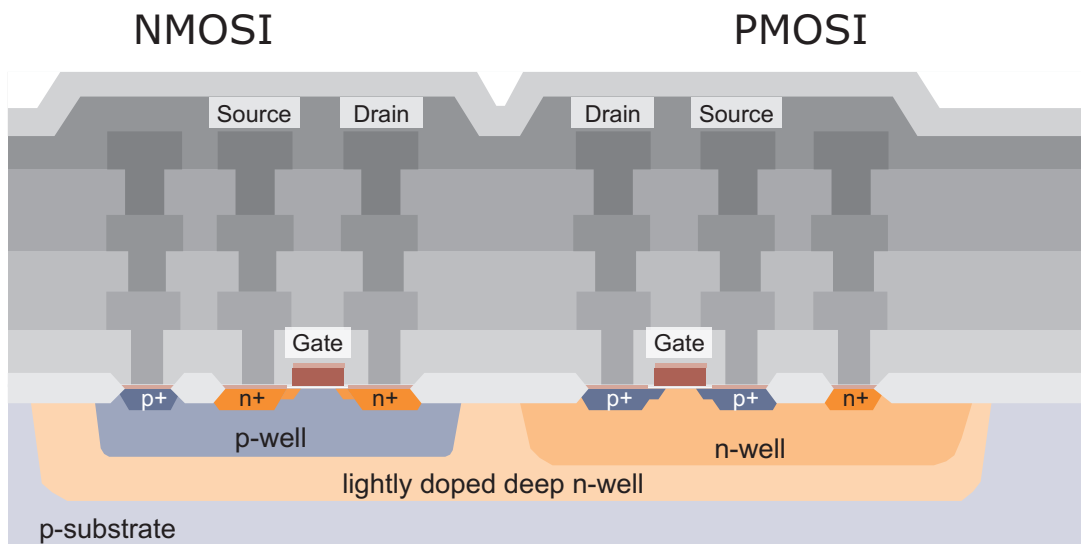


Figure 2: ISOMOS cross-section

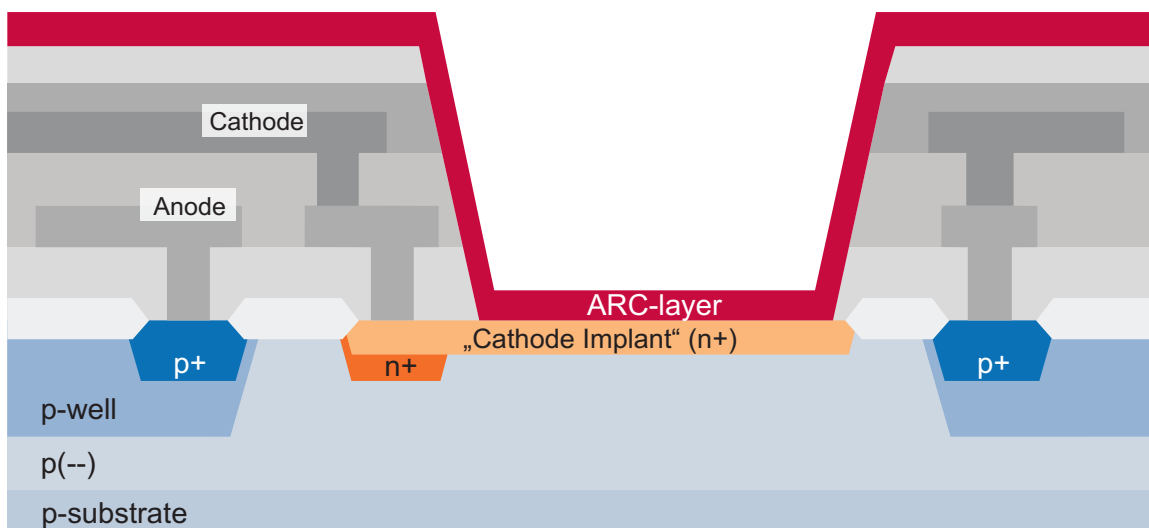


Figure 3: PIN diode cross-section

> Basic Design Rules

Mask	width [ $\mu\text{m}$ ]	Spacing [ $\mu\text{m}$ ]
N-well	1.6	7.0
Active area	0.5	0.6
Poly-silicon gate / resistor	0.35	0.45
Contact	0.4	0.4
Metal 1	0.5	0.45
Via 1 / 2 / 3	0.5	0.45
Metal 2 / 3	0.6	0.5
Top Metal 3 / 4	0.6	0.6
Opto	4.0	3.0

> Device Parameters

The following devices can be used for circuit designs. They are well characterized and part of a primitive device library. The device names correspond with the SPICE model names.

Different reliability tests gave the maximum allowed operating conditions; Values in brackets denote absolute maximum ratings. See also the availability with different options.

**Active Devices** (typical data)

MOS Transistor								
Device	Device Name	Available with module	VT  [V]	IDS [ $\mu\text{A}/\mu\text{m}$ ]	BVDS  [V]	Ioff [log(A/ $\mu\text{m}$ )]	max. VDS [V]	max. VGS [V]
3.3V NMOS	nmos	MOS	0.61	500	> 5.5	-13.0	3.6	3.6
3.3V PMOS	pmos	MOS	0.74	250	> 5.5	-13.0	3.6	3.6
Isolated 3.3V NMOS	nmosi	ISOMOS	0.59	500	> 5	-12.5	3.6	3.6
Isolated 3.3V PMOS	pmosi	ISOMOS	0.78	240	> 5	-14.0	3.6	3.6
5V NMOS	nmos5	MOSSA	0.91	450	> 7	-14.3	5.5	5.5
5V PMOS	pmos5	MOSSA	0.86	205	> 7	-14.7	5.5	5.5
Isolated 5V NMOS	nmos5i	MOSSA+ISOMOS	0.91	465	> 7	-14	5.5	5.5
Isolated 5V PMOS	pmos5i	MOSSA+ISOMOS	1.01	190	> 7	-15.7	5.5	5.5
12V drain NMOS	nha	MOS	0.59	97	> 15	-14	12	3.6

RF MOS Transistor							
Device	Device Name	Available with module	f <sub>T</sub> [GHz]	f <sub>max</sub> [GHz]	max. VDS [V]	max. VGS [V]	
3.3V RF NMOS	nmosrf	MOS	25	40	3.6	3.6	
3.3V RF PMOS	pmosrf	MOS	15	24	3.6	3.6	
3.3V isolated RF NMOS	nmosirf	ISOMOS	25	40	3.6	3.6	
3.3V isolated RF PMOS	pmosirf	ISOMOS	15	24	3.6	3.6	
5V RF NMOS (mid. ox.)	nmos5rf	MOSSA	14	36	5.5	5.5	
5V RF PMOS (mid. ox.)	pmos5rf	MOSSA	7.5	20	5.5	5.5	
5V isolated RF NMOS (mid. ox.)	nmos5irf	MOSSA+ISOMOS	14	36	5.5	5.5	
5V isolated RF PMOS (mid. ox.)	pmos5irf	MOSSA+ISOMOS	7.5	20	5.5	5.5	

Bipolar Transistor								
Device	Device Name	Available with module	BETA	VA [V]	VBE [mV]	BVCEO [V]	f <sub>T</sub> [GHz]	max. VCE [V]
vertical PNP 8 $\mu\text{m}^2$ emitter <sup>b)</sup>	qp1	MOS	4.5	190	720	-	-	3.6
lateral PNP	qpa	MOS	27	4.2	730	-	-	3.6
isolated vertical NPN	qnvb	MOS+ISOMOS	35	90	685	> 7	2.0	5.5
isolated vertical NPN	qnvc	MOSSA+ISOMOS	55	50	685	12	2.0	5.5

<sup>b)</sup> please refer to device models document for data for qp2 (155 $\mu\text{m}^2$  emitter), qp3 (12.5  $\mu\text{m}^2$  emitter), and qp4 (100 $\mu\text{m}^2$  emitter).

Device Parameter (continued)						
Photo Diodes						
Device	Device Name	Available with module	Cut off freq. [MHz]	Area cap. [fF/ $\mu\text{m}^2$ ]	Sensitivity [A/W]	Breakdown Voltage [V]
PIN (optimized for blue light)	dpinb	PINBLUE	750 @405nm <sup>o)</sup>	0.014	0.30 @405nm	> 50
PIN (with ARC optimized for red light)	dpinbr	PINBLUE	720 @650nm <sup>o)</sup>	0.014	0.52 @650nm	> 50
PIN (with ARC optimized for infra-red light)	dpinbir	PINBLUE	85 @844nm <sup>o)</sup>	0.014	0.40 @850nm	> 50
PIN (metal covered)	dpinb0	PINBLUE	-	0.014	-	> 50

<sup>o)</sup> diode size 100 x 100  $\mu\text{m}^2$

### Passive Devices (typical data)

Resistors and Conductors							
Device	Device Name	Available with module	RS [ $\Omega/\square$ ]	Thickness/Junction depth [ $\mu\text{m}$ ]	max. J/W [m $\mu\text{m}$ ]	Temp. coeff. [ $10^{-3}/\text{K}$ ]	max. VTB [V]
Polysilicon 1 silicided	rsp1	MOS	4.5	0.30	2	3.4	18
polysilicon 1	rp1	MOS	45	0.30	2	0.8	18
N+ HRES polysilicon	rnp1	HRPOLY	1000	0.30	2	-2.8	18
P+ HRES polysilicon	rpp1	HRPOLY	500	0.30	2	-0.5	18
Polysilicon 2	rp2	CAPPOLY	100	0.25	2	0.6	18
Poysilicon 2 silicided	rsp2	CAPPOLY	2.6	0.25	2	-	18
Low TCR polysilicon 2	rzp2	CAPPOLY	200	0.25	2	-0.2	18
P+ diffusion silicided	rsp	MOS	3.40	0.21	-	3.7	0
P+ diffusion in N-well	rdp rdp_io <sup>d)</sup>	MOS	150	0.21	-	1.6	0
P+ diffusion (DW)	rdplw rdplw_io <sup>d)</sup>	ISOMOS	143	-	-	1.6	0
N+ diffusion silicided	rsn	MOS	3.4	0.17	-	3.5	6
N+ diffusion in P-well	rdn rdn_io <sup>d)</sup>	MOS	85	0.17	-	1.6	6
N+ diffusion (DW)	rdnlw rdnlw_io <sup>d)</sup>	ISOMOS	85	-	-	1.6	6
N-well	rw	MOS	1160	1.1	-	3.9	6
Metal 1	rm1	MOS	0.090	0.58	1.0	3.4	18
Metal 2	rm2	MOS	0.090	0.58	1.0	3.4	18
Metal 3	rm3 rm3t	METAL4 MOS	0.090 0.043	0.58 1.00	1.6	3.4	18
Metal 4	rm4	METAL4	0.043	1.00	-	3.4	18

<sup>d)</sup> These devices should be used only as ESD protection resistors in IO-cells.

Capacitors							
Device	Device Name	Available with module	Area Cap. [fF/ $\mu\text{m}^2$ ]	Perimeter cap. [fF/ $\mu\text{m}$ ]	Linearity [ppm/V]	BV [V]	max. VTB [V]
POLY1-POLY2	cpp	CAPPOLY	0.85	0.021	-120	> 26	18
POLY1-POLY2, 2 terminal	cpp2	CAPPOLY	0.85	0.021	-120	> 26	18
MIM metal2/metal3, 3 terminal/ 2 terminal	cmm / cmm2	MIM	1.25	0.11	35	> 20	18
Double MIM, 3 terminal/ 2 terminal	cdmm / cdmm2	DMIM	2.5	0.22	35	> 20	18

> Device Parameter (continued)

**Passive Devices** (typical data) (continued)

Sandwiched Capacitors							
Device	Device Name	Available with module	Cap. [fF]	Voltage Coef. [1/V]	Temp. Coef [ppm/K]	BV [V]	max. VCC [V]
Polysilicon1/metal1/metal2/metal3	csandwt	MOS	135	-	-	-	18
Poly1/M1/M2/M3 finger	csandwtf	MOS	255	-	-	-	18
Poly1/M1/M2/M3/M4	csandwtm	METAL4	294	-	-	-	18

Stacked Capacitors		
Device	Available with module	Area Cap. [fF/μm <sup>2</sup> ]
cmm2 on cpp	MIM+CAPPOLY	2.0
cdmm2 on cpp	DMIM+CAPPOLY	2.6

Diodes						
Device	Device Name	Available with module	Area Cap. [fF/μm <sup>2</sup> ]	BV [V]	Area leakage current [fA/μm <sup>2</sup> ]	Sidewall leakage current [fA/μm]
N+ diffusion/ P-well	dn	MOS	0.790	> 7	4.0 x 10 <sup>-4</sup>	1.0 x 10 <sup>-3</sup>
P+ diffusion/ N-well	dp	MOS	0.810	> 7	5.0 x 10 <sup>-4</sup>	1.0 x 10 <sup>-3</sup>
5V N-well/ P-sub	dw	MOS	0.026	> 20	4.0 x 10 <sup>-4</sup>	2.0 x 10 <sup>-3</sup>
18V N-well/ P-sub	dwmv	MOS	0.026	> 20	4.0 x 10 <sup>-4</sup>	2.0 x 10 <sup>-3</sup>
P+ diffusion/ lightly doped deep Nw	dplw	ISOMOS	0.240	> 7	2.0 x 10 <sup>-4</sup>	1.0 x 10 <sup>-3</sup>
P-well/ lightly doped deep N-well	dwplw	ISOMOS	0.240	> 22	5.0 x 10 <sup>-4</sup>	1.0 x 10 <sup>-3</sup>
Lightly doped deep N-well/ P-sub	dlw	ISOMOS	0.038	> 22	1.0 x 10 <sup>-3</sup>	3.0 x 10 <sup>-2</sup>

Varactors						
Device	Device Name	Available with module	Tuning range [%]	Capacitance per length @0V, 100kHz [fF/μm]	Capacitance per length @2V, 100kHz [fF/μm]	Quality factor @ 1GHz
Diode	dpvc	MOS	36	4.4	2.8	35
Device	Device Name	Available with module	Tuning range [%]	Capacitance @+1V, 100kHz [fF/μm]	Capacitance @-1V, 100kHz [fF/μm]	Quality factor @ 1GHz
Accumulation mode	mosvc	MOS	71	3.5	1.0	50

Programmable Device						
Device	Device Name	Available with module	Reverse voltage [V]	Reverse voltage for fused device [V]	Voltage Temp. Coef [V/K]	Max. Iread [mA]
Zener Zap	dzap	MOS	4	0.05	6	0.05

Programmable Device						
Device	Device Name	Available with module	Unprogrammed resistance [Ω]	Programmed resistance [kΩ]	Programmed Max Vterm1-term2 [V]	unprog. Max Vterm1-term2 [V]
Poly fuse	pfuse	MOS	< 160	> 100	3.6	0.2

> Digital Core Library Cells

X-FAB provides three different core libraries optimized for most typical applications in mixed signal ASIC:

Name	Category	Density <sup>1)</sup>	r_factor <sup>2)</sup>	Main feature
D_CELLSL_HD	low power, high density	ML4: 28.0 ML3: 25.5 ML2: 11.0	ML2: 1.10 ML3: 1.20 ML4: 2.80	low power consumption, min. area
D_CELLSL_HDJI	low power, high density, junction isolated	ML4: 28.0 ML3: 25.5 ML2: 11.0	ML4: 1.10 ML3: 1.20 ML2: 2.80	low power consumption, junction isolated, low noise, voltage shifting, min. area
D_CELLSL_5V	low power, 5V, high density	ML4: 22.5 ML3: 20.5 ML2: 9.0	ML4: 1.10 ML3: 1.20 ML2: 2.80	low power consumption, 5V supply voltage

<sup>1)</sup> average value: kGE/mm<sup>2</sup> (GE = NAND2 Gate Equivalent)  
ML2: 2 metal layer routing, ML3: 3 metal layer routing, ML4: 4 metal layer routing

<sup>2)</sup> average value: r\_factor = Routing\_factor  
Place&Route\_area = Cell\_area \* Routing\_factor

> Digital I/O Cells

The digital I/O libraries contain a comprehensive range of I/O cells divided into distinct inputs, outputs and bidirectionals with variants for single voltage and dual voltage devices.

The digital I/O library has the following features:

Name	Category	Main feature
IO_CELLS	single voltage ( $V_{IO} = V_{CORE}$ )	Pad limited ( $x < y$ )
IO_CELLS_F	single voltage ( $V_{IO} = V_{CORE}$ )	Core limited ( $x > y$ )
IO_CELLS_F5V	5V supply multivoltage	core limited ( $x > y$ )

- I/O cells are optimized for 5V operating voltage and are fully functional down to 1.8V with derated output current and speed.
- Cell height for pad limited I/O cells is 424.2µm and minimum pad pitch is 89.6µm for cells occupying one pad location
- Cell height for core limited I/O cells is 248.8µm and minimum pad pitch is 173µm
- The TTL and CMOS level detection circuits use low noise power rails
- Outputs are available with selectable speeds to maintain low noise independent from DC output drive and can be configured as tri-state, bi-state, open drain or open source
- The core can be operated at lower voltage than the I/O cells
- 5V tolerant I/O cells are available.

	Pad Limited I/O Cells	Core Limited I/O Cells
Input	CMOS or TTL Level	CMOS or TTL Level
Schmitt Trigger Cells CMOS/TTL	■/■	■/■
<b>Input Option</b>	Gated Pull-up	■
	Gated Pull-down	■
	Input Hold	■
	Gated CMOS Input	■
	NAND Tree	■
Output	Tri-state Output	Tri-state Output
Output Drive	2, 6, 12, 24mA	2, 6, 12mA
Slew Rate Control	■	■
Configurations	Bi-state Output Tri-state Output Open Drain Output Open Source Output	Bi-state Output Tri-state Output Open Drain Output Open Source Output
<b>Cell Size</b>	Cell Height	424.20.0µm
	Cell Width / Pad Pitch	x2, x6, x12 cells 89.6µm x24 cells 156.8µm
ESD Robustness	4kV (HBM)	2kV (HBM)

> RFCMOS I/O Pad Libraries

The RFCMOS I/O pad libraries has the following features:

- RFCMOS I/O pad libraries contain analog RF I/O cells, digital input and digital output cells.
- Analog RFCMOS I/O cells are available in variant with different ESD protection structures providing higher ESD level or lower pad capacitance as well as different series resistances.
- RFCMOS digital input cells are available with non-inverting input buffer for different speeds or Schmitt trigger input, both with gated pull-down and pull-up option
- RFCMOS digital output cells are available with tri-state output and 2, 4, or 8mA drive strength
- All RFCMOS pad cells have a cell height of 210µm and a cell width of 120µm

> Analog Primitive Devices and Models

A very wide range of different analog primitives enable analog and RF designers to develop sophisticated, high precision, reliable analog and high voltage circuits. See section “Device Parameters” for details.

High performance process modules, well-defined primitives devices and accurate device models are the key success factors for analog, RF and mixedsignal design. Combined with X-FAB’s CAE support kit “TheKit” and state of the art design methodologies, right first time analog, RF and mixedsignal designs can be realised.

X-FAB supports the latest BSIM3v3 models as the present SPICE model standard for MOS transistors. RF MOS transistors are modeled as subcircuit based on BSIM3v3 core with parasitics included. Bipolar transistors are modeled using the Gummel-Poon model for a given emitter size. Well resistors have

a non-linear terminal-voltage and bulk-voltage dependence. These resistances have to be simulated with the 3-terminal SPICE JFET model. High frequency MOS and diode varactors are modeled with three-terminal subcircuit including parasitic resistors, capacitors and diodes.

Model sets for most popular analog simulators, e.g. Spectre, HSPICE and PSPICE are provided. The same characterization and modeling effort is spent for parasitic devices and 3rd order parameters, which are usually very important for analog design.

The matching behavior of MOS transistors, bipolar transistors, resistors and capacitors is investigated and characterized. Final matching parameters are extracted for all active and most passive elements.

> Examples for measured and modeled parameter characteristics

CMOS and Bipolar transistor Output Characteristics typical data)

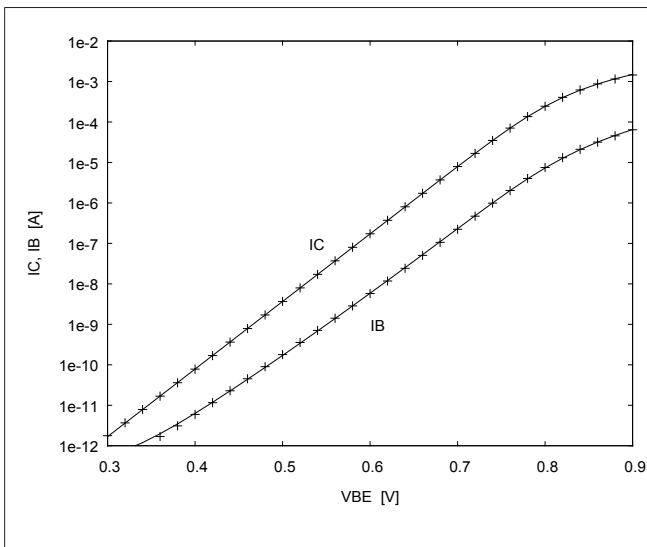


Figure 4: Device qnvb: gummel plot of vertical NPN bipolar transistor for a typical wafer. LE = 10µm, VCB = 0V, + = measured, solid line = SPICE model

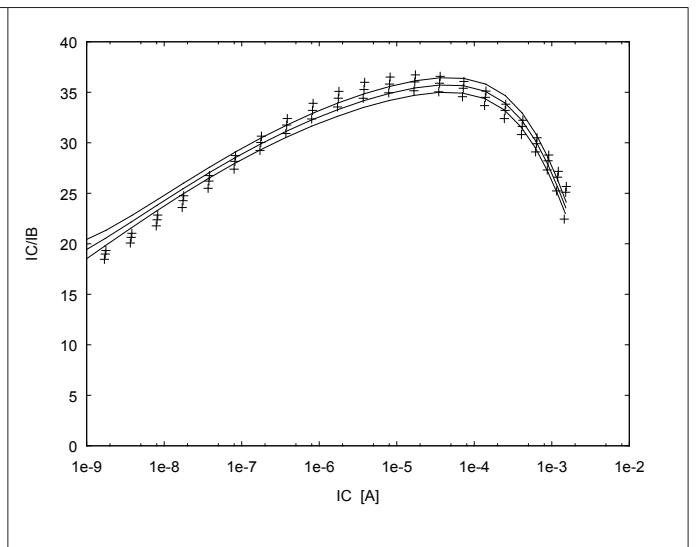


Figure 5: Device qnvb: current gain of vertical NPN bipolar transistor for a typical wafer. LE = 10µm, VCB = 0, 1.5, 3V, + = measured, solid line = SPICE model

Examples for measured and modeled parameter characteristics

CMOS and Bipolar transistor Output Characteristics typical data) (continued)

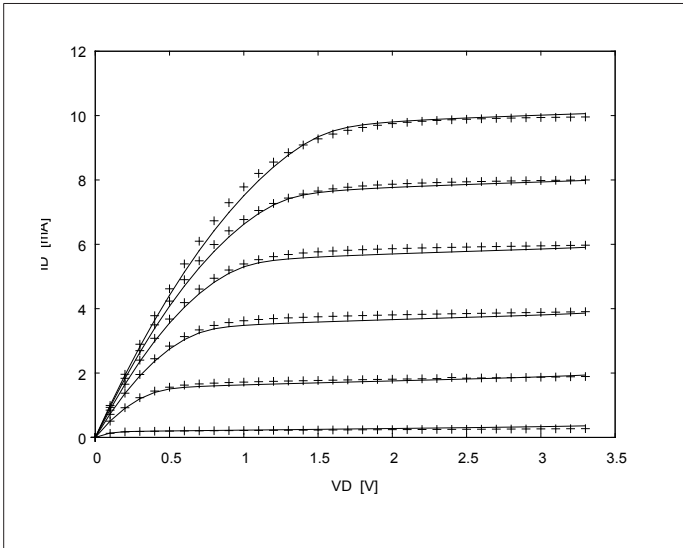


Figure 6: Device nmos: output characteristic of a typical wafer, W/L = 20/0.35, VGS = 1.2, 1.8, 2.4, 3.0, 3.6V dotted line = measured, solid line = simulated

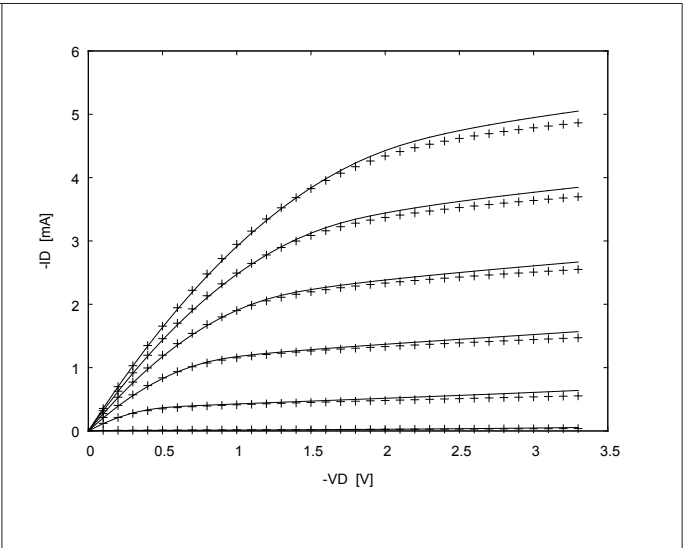


Figure 7: Device pmos: output characteristic of a typical wafer, W/L = 20/0.35, VGS = 1.2, 1.8, 2.4, 3.0, 3.6V dotted line = measured, solid line = simulated

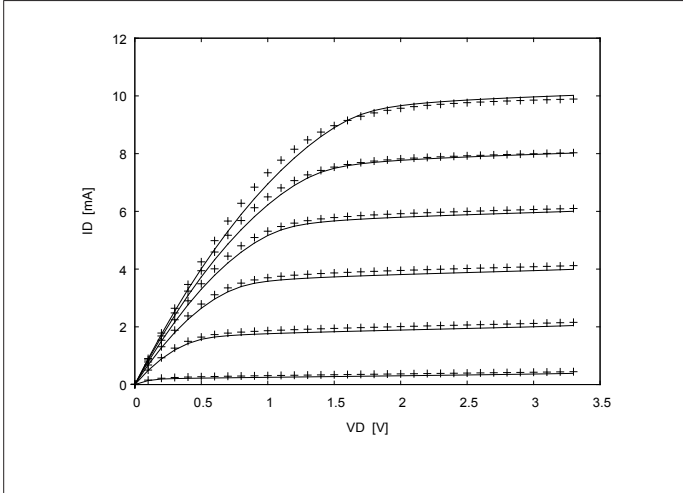


Figure 8: Device nmosi: output characteristic of a typical wafer, W/L = 20/0.35, VGS = 1.2, 1.8, 2.4, 3.0, 3.6V dotted line = measured, solid line=BSIM3v3

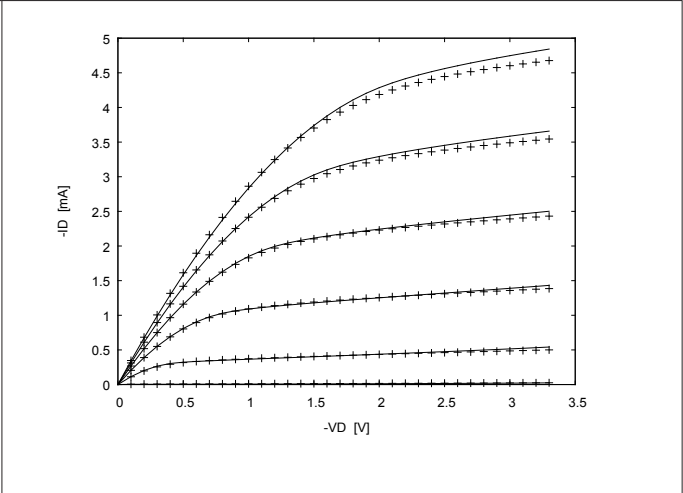


Figure 9: Device pmosi: output characteristic of a typical wafer, W/L = 20/0.35, -VGS = 0.8, 1.3, 1.8, 2.3, 2.8, 3.3V, + = measured, solid line = BSIM3v3 model

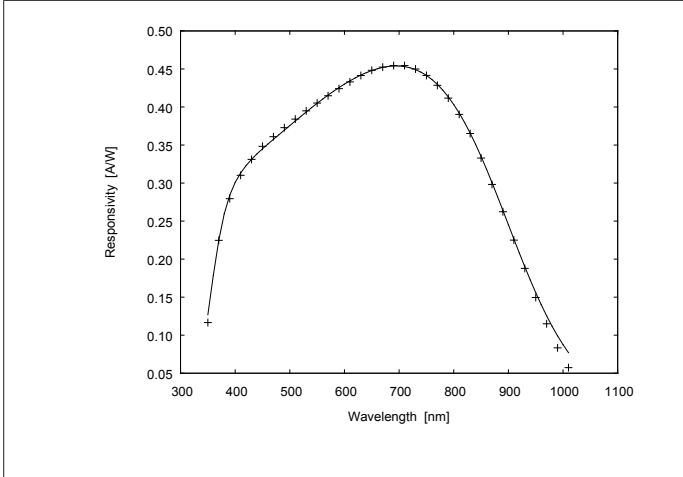


Figure 10: Device dpinb: responsivity vs. wavelength plot

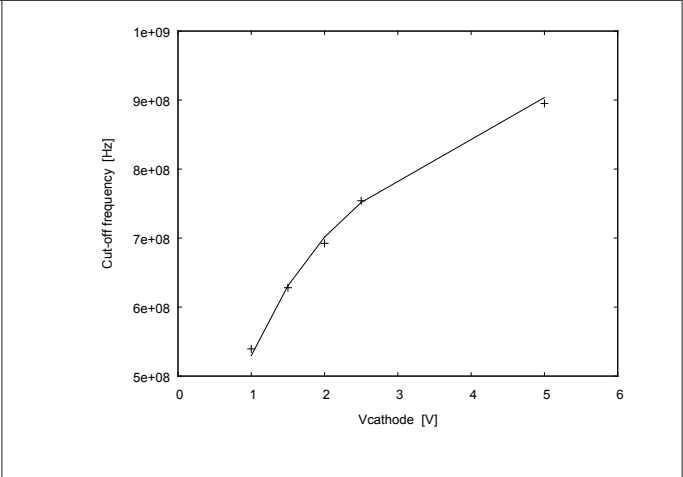
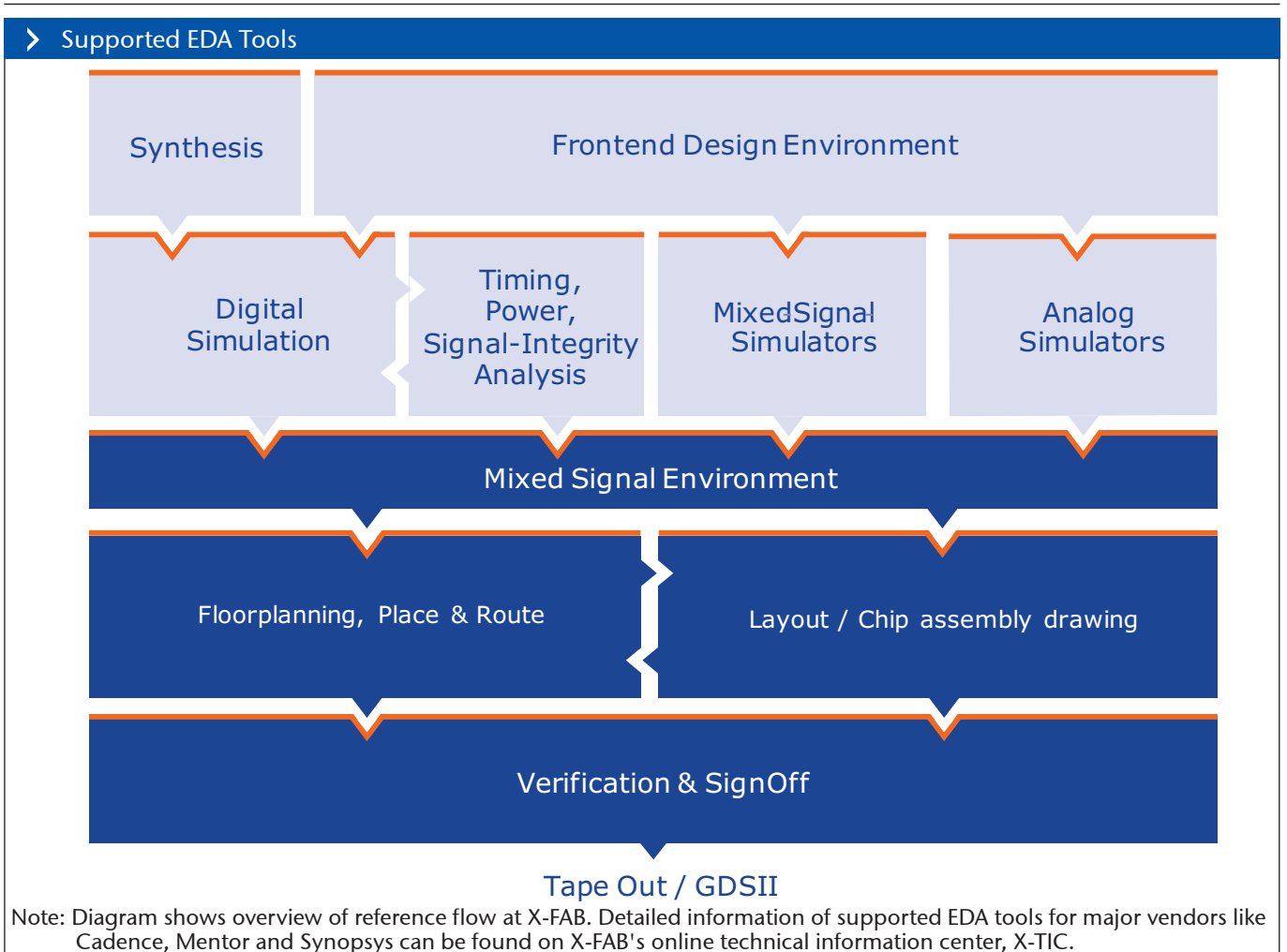


Figure 11: Device dpinb: Cut-off frequency vs. cathode voltage for a typical wafer, W=L=100µm, wavelength = 400nm, + = measured, solid line = model



> X-FAB's IC Development Kit "TheKit"

The X-FAB IC Development *Kit* is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-end and back-end

information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well.

The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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