

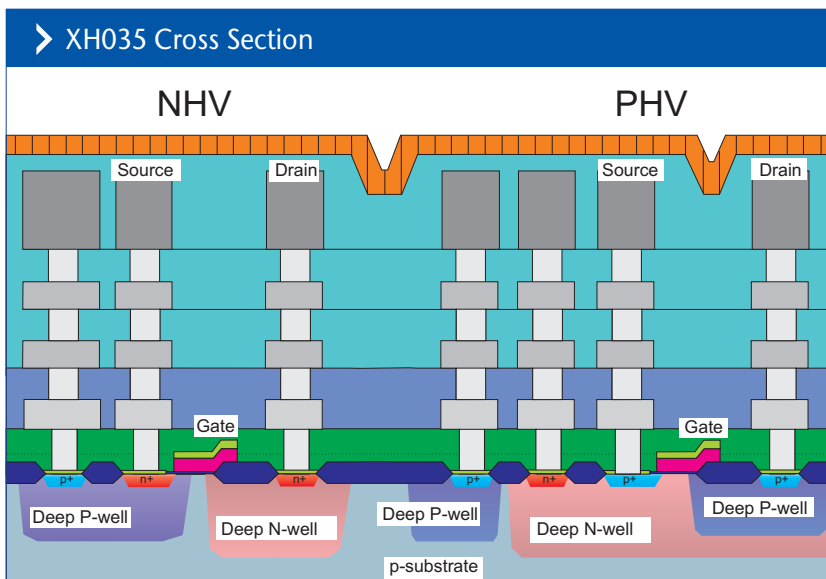
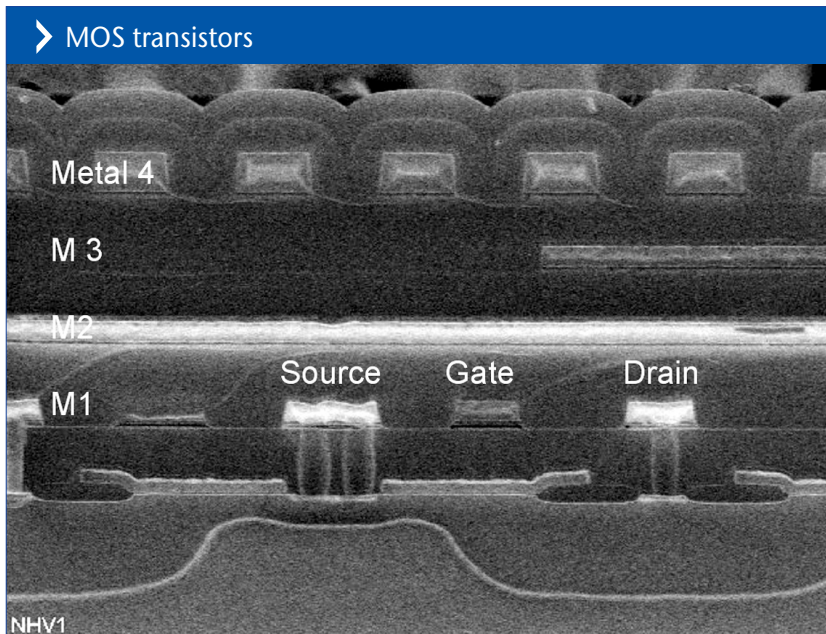
# 0.35 $\mu\text{m}$ CMOS Process Family

## > XH035

### Analog and High Voltage Options with Non Volatile Memory

> Modular 0.35  $\mu\text{m}$  CMOS process with 4 different process cores for analog/mixed-signal and high voltage applications.

The selected core can be combined with front end of line (FEOL) and back end of line (BEOL) options to create variety of active and passive elements, RF components and embedded EEPROM.



### > Module Overview

#### Cores

- MOS**  
Core MOS module
- MOSLT**  
Low threshold MOS module
- MOSLL**  
Low leakage MOS module
- MOSS**  
Mid gate oxide MOS module

#### FEOL Options

- MOSSA**  
Mid gate oxide module
  - ISOMOS**  
Isolated N-/PMOS module
  - THKOX**  
Thick gate oxide module
  - NMVMOS**  
Medium voltage NMOS module
  - PMVMOS**  
Medium voltage PMOS module
  - DEPL**  
Depletion NMOS module
  - BURDIF**  
Buried N module
  - CAPPOLY**  
Polysilicon 2 module
  - LRPOLY**  
Low resistance polysilicon
  - HRPOLY**  
High resistance polysilicon
  - XRPOLY**  
Very high resistance polysilicon
  - EEPROM**  
EEPROM module
- #### BEOL Options
- MIM**  
MIM capacitor module
  - DMIM**  
Double MIM capacitor module
  - METAL2**  
Top metal 2 module
  - METAL4**  
Metal 4 module
  - THKMET**  
Thick metal 4 module

# 0.35 μm CMOS Process

## > XH035

### with Embedded Non Volatile Memories and High Voltage Options

- Compatible with state of the art 0.35 μm – 3.3V – CMOS
- Low leakage (MOSLL) and low threshold (MOSLT) voltage option
- Optional triple well isolation for 3.3V CMOS
- Optional 5V single gate or 5V dual gate oxide for 5V operation
- Wide range of medium and high voltage MOS transistors with BV >50V
- HV NMOS & PMOS devices with low RDSon
- Thin gate oxide HV transistor for power management applications
- Very high poly resistor (10kΩ/□) module
- Suitable for 14V automotive board net
- Bipolar transistors for different voltages
- Embedded EEPROM with high endurance
- Passive elements for analog and RF applications
- MIM, double MIM or stacked MIM and PIP capacitors
- 2, 3 or 4 metal layers possible
- Thick top metal

Design Rules	
Parameter	Pitch [μm]
Polysilicon 1	0.8
Active area	1.1
N-Well	2.6
Metal 1 (contacted)	1.15
Metal 2, 3 (contacted)	1.4
Metal 4 (contacted)	1.4
Contact	0.8
Via 1, 2, 3	0.95

Resistors	
Device	Sheet Resistance [Ω/□]
N+ diffusion	85
P+ diffusion	143
N-well	1160
Poly1	40
Poly2 (low TC)	200
Poly1 (high res)	1000
Poly1 (xhigh res)	10000

Transistors Parameters				
Device	Vt  [V]	BVDSS  [V]	IDS  [μA/μm]	loff  [pA/μm]
NMOS 3.3V	0.60	> 5	500	0.2
NMOS_LT	0.55	> 5	485	1.0
NMOS_LL	0.67	> 5	430	0.02
PMOS 3.3V	0.74	> 5	250	0.2
PMOS_LT	0.50	> 5	240	0.2
PMOS_LL	0.73	> 5	190	0.002
Device	Vt  [V]	BVDSS  [V]	IDS  [μA/μm]	RDSon [mΩmm²]
NMOS 14V	1.02	> 20	300	50
PMOS 14V	0.95	> 20	170	135
NMOS 45V	0.90	> 50	320	97
PMOS 45V	0.88	> 50	140	369

Capacitors		
Device	Area Cap [fF/μm²]	Max. VCC [V]
poly1-poly2 (PIP)	0.85	10
poly1-met1-2-3-4	0.25	45
poly1 on diffusion (POD)	4.0	3.6
poly1 on diffusion (hv)	0.85	18
metal-isolator-metal (MIM)	1.25	45
double MIM	2.50	45
stacked PIP & POD	4.85	3.6



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