0.18 µm CMOS Process

XC018

MIXED-SIGNAL FOUNDRY EXPERTS

0.18 Micron Modular RF enabled CMOS Logic and Analog Technology

Description

The XC018 series is X-FAB's 0.18 micron Modular Logic and Mixed Signal Technology. The platfrom is ideal for SOC application. Main target applications are standard cell, semi-custom and full custom designs for Automotive, Consumer, Industrial as well as Telecommunication products, while the low power and high voltage process is ideal for mobile applications as well as display drivers or controllers. Based upon the industrial standard single poly with up to six metal layers 0.18-micron drawn gate length N-well process, modules are also available for metal-insulator-metal capacitors, high resistive poly, dual gate oxide (1.8V with 3.3V or 5.0V) transistors.

Comprehensive design rules, precise SPICE models, analog and digital libraries, IP's and development kits support the process for major EDA vendors.

Key Features

- 1.8V logic layout & performance compatible with the industry standard
- 0.18-micron single poly, up to six-metal N-well CMOS basic process
- Modular concept
- Standard & Low Power modules
- 1.8V core with 3.3V or 5.0V I/O option
- Salicided Source & Drain
- Direct STI
- Isolation well for all 1.8V, 3.3V & 5.0V MOS devices
- High value poly resistor
- Metal-Insulator-Metal capacitors
- **NEW**: Double MIM & Triple MIM Capacitors
- **NEW**: I/O cell library with 4kV HBM ESD protection levels
- **NEW**: RF characterisation and models for all RF MOS transistors and passive components
- **NEW**: Thick top metal for inductors and Smart Power applications
- Gate oxide thickness: 5.0V -125Å, 3.3V - 60Å, 1.8V - 30Å
- High Density up to 115000 gates per mm²
- Typical and worst-case models - BSIM3v3.24 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterised & included in model
- Calibre & Assura verification deck
- Cadence PDK

Applications

- Standard Logic/Controller circuits
- Mixed signal embedded systems/ systems on a chip (SOC)
- High Precision mixed signal circuits
- Low power mixed signal circuits
- Analog front ends for sensors
- Embedded High Voltage applicaitons
- RF Applications
- Communications, Consumer, Automotive and Industrial markets

Quality Assurance

X-FAB spends a lot of effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS 16949 and other standards.

Deliverables

- PCM tested wafers
- Optional production services: wafer sort
- Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development

Digital Libraries

- Foundry-specific optimized libraries
- Standard core library for high speed digital blocks
- Low Power library for energy effecient and small size digital blocks
- IEEE 1364 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models

Primitive Devices

- NMOS/PMOS Transistors (1.8V, 3.3V & 5.0V)
- Bipolar Transistors
- Diodes
- Capacitors
- Resistors
- Varactors
- Inductors

Process Modules

Module Name	Number of Masks	Remarks	Typical Primitive Devices Applications
MOSLP	17	Low Power MOS module Single Poly, Triple Metal	1.8V NMOS/PMOS & resistor
MOSST	17	Standard MOS module Single Poly, Triple Metal	1.8V NMOS/PMOS & resistor

To get the available technology options, this main module can be combined with one or moreof the following additional modules:

Module Name	Number of Additional Masks	Remarks	Typical Primitive Devices Applications
MOS3LP [a]	5	Low power 3.3V CMOS module, additional gate oxide, N-well & P-well	3.3V low power NMOS/PMOS 3.3V Native NMOS, I/O cells lbrary
MOS3ST [a]	3	Standard 3.3V CMOS module, additional gate oxide	3.3V standard NMOS/PMOS 3.3V Native NMOS, I/O cells library
MOS5LP [a]	5	Low power 5.0V CMOS module, additional gate oxide, N-well & P-well	5.0V low power NMOS/PMOS I/O cells library
MOS5ST [a) b)]	5	Standard 5.0V CMOS module, additional gate oxide, N-well & P-well	5.0V standard NMOS/PMOS I/O cells library
ISOMOS [a]	2	Triple wells isolated CMOS module	Isolated 1.8V, 3.3V or 5.0V CMOS for substrate noise suppression
HRPOLY	1	High resistance poly-silicon module	High value poly-silicon resistor
MIM	1	Single MIM capacitor module	Single MIM capacitor
DMIM	1	Double MIM capacitor module	Double MIM capacitor
TMIM	1	Triple MIM capacitor module	Triple MIM capacitor
4METALS	2	4 metal module	More complex wiring
5METALS [a]	2	5 metal module	More complex wiring
6METALS [a]	2	6 metal module	More complex wiring
THKMET [a]	2	Thick metal module, additional think metal & thick via module	Power distribution, inductors
PIMIDE	1	Polyimide module, resilient barrier layer on top of passivation	Wafer overcoat for stress relief and passivation protection

Notes: a) This module requires the addition of other modules or may not be used in combination with other modules!
b) MOS5ST module is under development.

Module name	Use of module also requires use of the following module	Combination not possible with the following module
MOSLP		MOSST, MOS3ST, MOS5ST
MOSST		MOSLP, MOS3LP, MOS5LP
MOS3LP	MOSLP	MOSST, MOS3ST, MOS5ST, MOS5LP
MOS3ST	MOSST	MOSLP, MOS3LP, MOS5LP, MOS5ST
MOS5LP	MOSLP	MOSST, MOS3LP, MOS3ST, MOS5ST
MOS5ST	MOSST	MOSLP, MOS3LP, MOS5LP, MOS5LP
ISOMOS	MOSST or MOSLP or MOS3ST or MOS3LP or MOS5ST or MOS5LP	
MIM		DMIM, TMIM
DMIM	4METALS	MIM, TMIM
TMIM	5METALS	MIM, DMIM
5METALS	4METALS	
6METALS	5METALS	THKMET
THKMET		6METALS

Main Process Flow

MOSST / MOSLP

Core Modules	Additional Modules	Module
Wafer Start		
	Zero Layer Oxide	ISOMOS
	HV Well Implant	THKOX
	DN Well Implant	THKOX/ISOMOSS
Active Area		
	HV Gate Oxide	THKOX
	HV PMOS Vt Adjust	NMVMOS
1.8V Wells		
	3.3V / 5V Wells	MOS3LP/MOS3ST/MOS5LP/MOS5ST
1.8V Gate Oxide		
	MV Gate Oxide	MOS3LP/MOS3ST/MOS5LP/MOS5ST
Poly 1		
1.8V NMOS LDD		
1.8V PMOS LDD		
	3.3V / 5V PMOS LDD 3.3V / 5V NMOS LDD	MOS3LP/MOS3ST/MOS5LP/MOS5ST
Source/Drain Imp.		
	High Resistance Poly	HRPOLY
Salicidation		
Contact		
Metal 1		
Via 1		
Metal 2		
Via 2		
	Double MIM Capacitor	DMIM
	Triple MIM Capacitor	TMIM
	Metal 3	4METALS
	Double MIM Capacitor	DMIM
	Triple MIM Capacitor	TMIM
	Via 3 Metal 4	5METALS
	Triple MIM Capacitor	TMIM
	Via 4 Metal 5	6METALS
	MIM Capacitor	Single MIM
Top Via		
Top Metal		
	Thick Metal Via Top Thick Metal	THKMET
Passivation		
	Polyimide	Polyimide
Wafer End		

Core Modules — Additional Modules

mask steps

Schematic Cross Sections

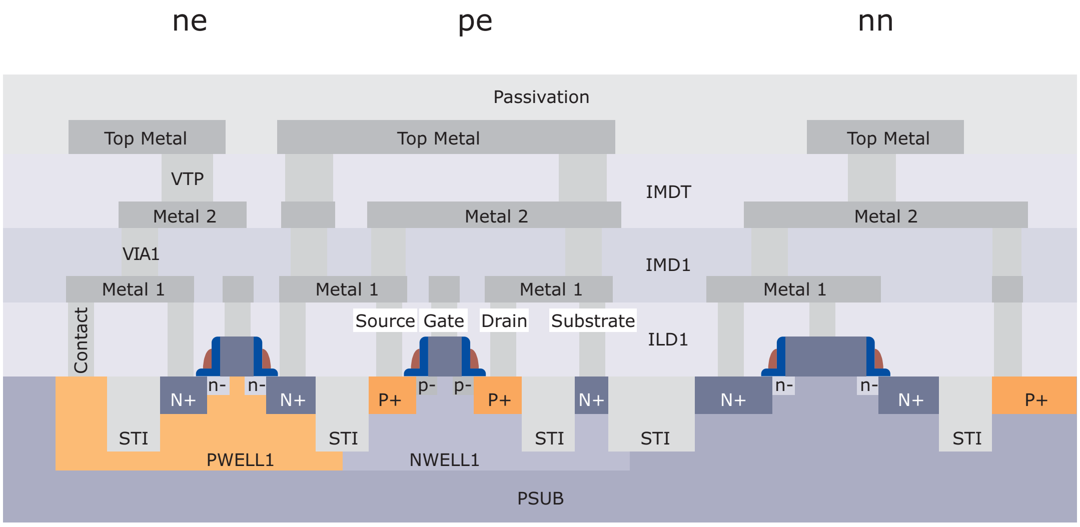


Figure 1: MOSST, MOSLP Module Transistors

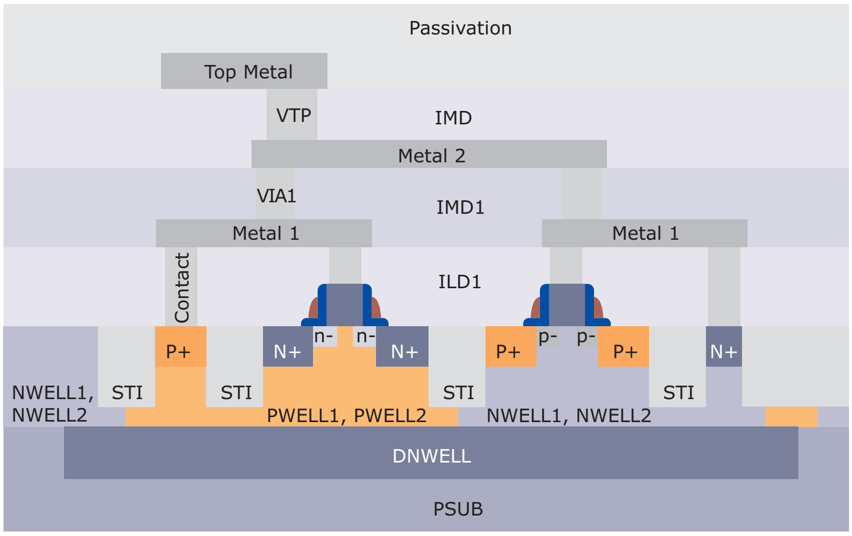


Figure 2: ISOMOS Module Transistors

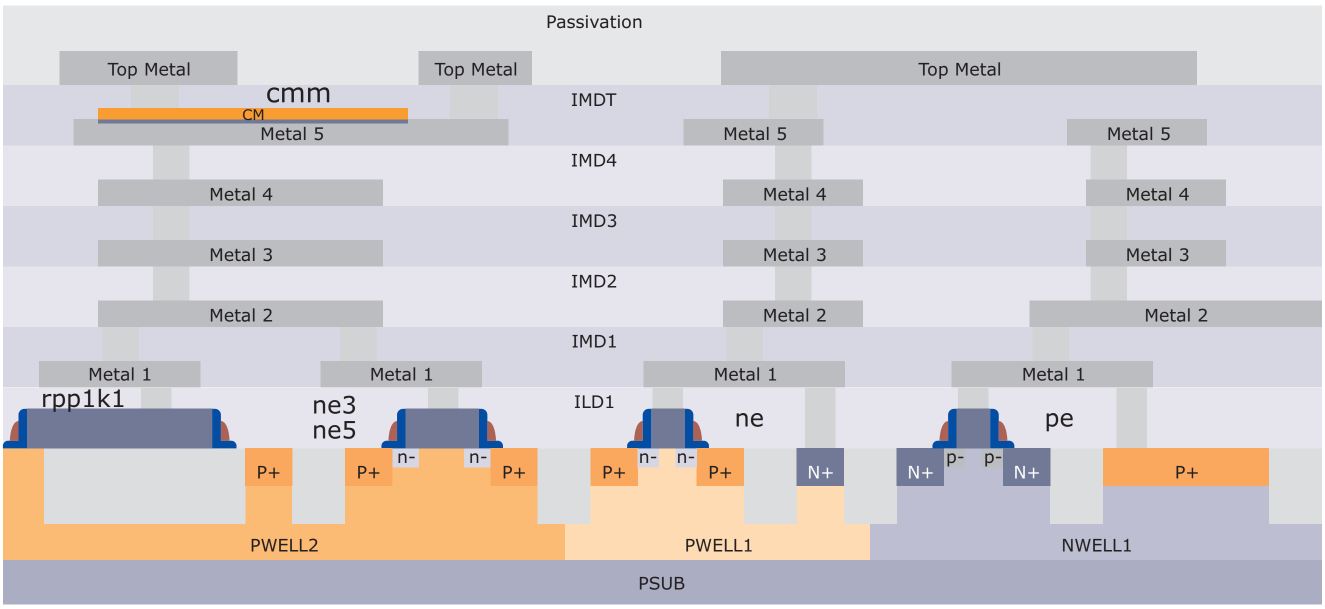


Figure 3: HRPOLY, 4METALS, 5METALS, 6METALS, MIM Module

Basic Design Rules

Mask	Width [µm]	Spacing [µm]
N-Well	0.86	1.4
Active Area	0.22	0.28
Poly-Silicon Gate	0.18	0.25
Poly-Silicon Resistor	0.44	0.44
Contact	0.22	0.25
Metal 1	0.23	0.23
Via 1/2/3/4	0.26	0.26
Metal 2/3/4/5	0.28	0.28
Top Via	0.36	0.35
Top Metal	0.44	0.46

Device Parameters

The following devices can be used for circuit designs. They are well characterized and part of a device library.

Active Devices (typical data)

MOS Transistors							
Device	Name	Available with module	|VT| [V]	IDS [µA/µm]	|BVDSS| [V]	Ioff [pA/µm]	Max. VDS, VGB [V]
Native Vt 1.8V NMOS*	nn	MOSLP, MOSST	-	-	-	-	-
1.8V NMOS	ne	MOSLP	0.60	480	> 4	< 3	1.98
		MOSST	0.43	620	> 4	< 50	
Isolated 1.8V NMOS	nei	MOSLP+ISOMOS	0.80	480	> 4	< 3	1.98
		MOSST+ISOMOS	0.43	620	> 4	< 50	
1.8V PMOS	pe	MOSLP	0.65	170	> 4	< 3	1.98
		MOSST	0.51	270	> 4	< 50	
Isolate 1.8V PMOS	pei	MOSLP+ISOMOS	0.65	170	> 4	< 3	1.98
		MOSST+ISOMOS	0.51	270	> 4	< 50	
Native Vt 3.3V NMOS*	nn3	MOSLP, MOSST	-	-	-	-	-
3.3V NMOS	ne3	MOS3LP	0.7	600	> 7	< 3	3.6
		MOS3ST	0.75	600	> 7	< 10	
Isolated 3.3V NMOS	ne3i	MOS3LP+ISOMOS	0.7	600	> 7	< 3	3.6
		MOS3ST+ISOMOS	0.75	600	> 7	< 10	
3.3V PMOS	pe3	MOS3LP	0.63	300	> 7	< 3	3.6
		MOS3ST	0.69	290	> 7	< 10	
Isolated 3.3V PMOS	pe3i	MOS3LP+ISOMOS	0.63	300	> 7	< 3	3.6
		MOS3ST+ISOMOS	0.69	290	> 7	< 10	
5.0V NMOS	ne5	MOS5LP	0.77	530	> 10	< 5	5.5
		MOS5ST*	-	-	-	-	-
Isolated 5.0V NMOS	ne5i	MOS5LP+ISOMOS	0.77	530	> 10	< 5	5.5
		MOS5ST+ISOMOS*	-	-	-	-	-
5.0V PMOS	pe5	MOS5LP	0.84	240	> 8.4	< 10	5.5
		MOS5ST*	-	-	-	-	-
Isolated 5.0V PMOS	pe5i	MOS5LP+ISOMOS	0.84	240	> 8.4	< 10	5.5
		MOS5ST+ISOMOS*	-	-	-	-	-

Notes: *) module still under development

Device Parameters *(continued)*

Active Devices (typical data) *(continued)*

RF MOS Transistors				
Device	Name	Available with module	f_T [GHz]	f_{max} [GHz]
1.8V NMOS for RF	nerf	MOSLP	50	75
Isolated 1.8V NMOS for RF	neirf	MOSLP+ISOMOS	50	75
1.8V PMOS for RF	perf	MOSLP	20	40
Isolate 1.8V PMOS for RF	peirf	MOSLP+ISOMOS	20	40
3.3V NMOS for RF	ne3rf	MOS3LP	27	57
Isolated 3.3V NMOS for RF	ne3irf	MOS3LP+ISOMOS	27	57
3.3V PMOS for RF	pe3rf	MOS3LP	15	30
Isolated 3.3V PMOS for RF	pe3irf	MOS3LP+ISOMOS	15	30
5.0V NMOS for RF	ne5rf	MOS5LP	18	48
Isolated 5.0V NMOS RF	ne5irf	MOS5LP+ISOMOS	18	48
5.0V PMOS for RF	pe5rf	MOS5LP	9	24
Isolated 5.0V PMOS RF	pe5irf	MOS5LP+ISOMOS	9	24

Bipolar Transistors						
Device	Name	Available with module	BETA	VA [V]	Max.VCE [V]	Max. VEB [V]
1.8V Vertical PNP	qpva/b/c	MOSLP	3.1	> 100	1.98	1.98
		MOSST	2.4	> 100	1.98	1.98
3.3V Vertical PNP	qpva/b/c3	MOS3LP	2.9	> 100	3.6	3.6
		MOS3ST	2.4	> 100	3.6	3.6
5.0V Vertical PNP	qpva/b/c5	MOS5LP	2.1	> 100	5.5	5.5
		MOS5ST	-	-	-	-

Passive Devices (typical data)

Capacitors*						
Device	Name	Available with module	Area Cap [fF/µm²]	BV [V]	Max. VCC [V]	Max. VTB [V]
single MIM		MIM	1.0	> 33	5.5	35
double MIM		DMIM	2.0	> 33	5.5	35
triple MIM		TMIM	3.0	> 33	5.5	35

*) In addition to the capacitors stated in the primitive device list it is also possible to use the capacitors built by the gate oxide or the mid oxide. These capacitors can be simulated by using the model of a transistor which has the respective oxide: for instance the ne and pe models in case of the 1.8V gate oxide.

The operating conditions of the relating transistors are valid as well for these capacitors

Inductors						
Device	Name	Available with module	Number of turns	Outer Diameter [µm]	Inductance [nH]	Q-Factor
Symmetric inductor for 2.4GHz	l24a	THKMET	4	270	3.8	15.6
Symmetric inductor for 5.0GHz	l50a	THKMET	4	200	2.0	12.9

Device Parameters *(continued)*

Passive Devices (typical data)

Resistors & Conductors							
Device	Name	Available with module	RS [Ω/☐]	Thicknes or junc. depth [µm]	Max J/W [mA/µm]	Temp. Coeff [10^{-3}/K]	Max. VTB [V]
N+ Poly*	rnp1	MOSLP, MOSST	330	0.11	1.0	-1.5	35
P+ Poly*	rpp1	MOSLP, MOSST	280	0.14	1.0	- 0.04	35
1.8V N+ diffusion resistor*	rdn	MOSLP, MOSST	62	0.25	-	1.4	1.95
1.8V P+ diffusion resistor*	rdp	MOSLP,MOSST	135	0.28	-	1.3	1.95
1.8V N-well	rnw	MOSLP, MOSST	970	0.66	-	3.0	5.5
3.3V N+ diffucion resistor*	rdn3	MOS3LP, MOS3ST	62	0.25	-	1.4	3.6
3.3V P+ diffusion resistor*	rdp3	MOS3LP, MOS3ST	135	0.28	-	1.3	3.6
3.3V N-well	rnw3	MOS3LP, MOS3ST	970	-	-	3.0	5.5
5.0V N+ diffusion resistor*	rdn5	MOS5LP, MOS5ST	62	0.25	-	1.4	5.5
5.0V P+ diffusion resistor*	rdp5	MOS5LP, MOS5ST	135	0.28	-	1.3	5.5
5.0V N-well	rnw5	MOS5LP, MOS5ST	970	-	-	3.0	5.5
High resistive Poly*	rpp1k1	HRPOLY	1000	1.9	1.0	-0.9	35
Metal 1	rm1	MOSLP, MOSST	0.095	0.17	1.0	3.2	35
Metal 2	rm2	MOSLP, MOSST	0.085	0.22	1.0	3.2	35
Top Metal	rmtp	MOSLP, MOSST	0.037	0.35	1.6	3.2	35
Metal 3	rm3	4METALS	0.085	0.25	1.0	3.2	35
Metal 4	rm4	5METALS	0.085	0.25	1.0	3.2	35
Metal 5	rm5	6METALS	0.085	0.25	1.0	3.2	35
Thick Matel	rmtpl	THKMET	0.012	3.0	6	3.5	35

*) non-salicided

Varactors						
Device	Name	Available with module	Area cap @ +1V [fF/µm^2]	Area cap @ -1V [fF/µm^2]	Max VGB [V]	Tuning Range @ -1~1V [%]
1.8V MOS varactor	mosvc	MOSLP, MOSST	8.2	3.5	1.95	57
3.3V MOS varactor	mosvc3	MOS3LP, MOS3ST	5.5	2.5	3.6	54
5V MOS varactor	mosvc5	MOS5LP, MOS5ST	2.71	1.5	5.5	45

RF Varactors						
Device	Name	Available with module	Area cap @ 0V 100kHz [fF/µm^2]	Area cap @2V 100kHz [fF/µm^2]	Tuning Range @ 0~1.8V [%]	Q @ 1 GHz
1.8V MOS varactor for RF	mosvcrf	MOSLP	-	-	57	50
3.3V MOS varactor for RF	mosvc3rf	MOS3LP	-	-	54	70
5V MOS varactor for RF	mosvc5rf	MOS5LP	-	-	45	140
1.8V diode varactor for RF	dpvcrf	MOSLP	0.98	0.66	33	60
3.3V diode varactor for RF	dpvc3rf	MOS3LP	1.0	0.66	34	60
5V diode varactor for RF	dpvc5rf	MOS5LP	0.96	0.64	33	60

Device Parameters *(continued)*

Passive Devices (typical data) *(continued)*

Diodes					
Device	Name	Available with module	Area junction cap [fF/µm^2]	Breakdown Voltage [V]	Max Vreverse [V]
1.8V N+ Diff. /P-well	dn	MOSLP, MOSST	1.12	> 9	1.95
1.8V P+ Diff. /N-well	dp	MOSLP, MOSST	0.98	> 9	1.95
1.8V N-well /P-sub	dnw	MOSLP, MOSST	0.12	> 15	5.5
3.3V N+ Diff. /P-well	dn3	MOS3LP, MOS3ST	0.87	> 9	3.6
3.3V P+ Diff. /N-well	dp3	MOS3LP, MOS3ST	1.00	> 9	3.6
3.3V N-well /P-sub	dnw3	MOS3LP, MOS3ST	0.12	> 15	5.5
5.0V N+ Diff. /P-well	dn5	MOS5LP, MOS5ST	1.07	> 10	5.5
5.0V P+ DIff. /N-well	dp5	MOS5LP, MOS5ST	0.96	> 9	5.5
5.0V N-well /P-sub	dnw5	MOS5LP, MOS5ST	0.13	> 15	5.5
DN-well /P-sub	ddnw	MOSLP, MOSST, ISOMOS	0.50	> 15	5.5
1.8V P-well /DN-well	dpw	(MOSLP/MOSST) +ISOMOS	0.70	-	5.5
3.3V P-well /DN-well	dpw3	(MOS3LP/MOS3ST) +ISOMOS	0.70	-	5.5
5V P-well /DN-well	dpw5	(MOS5LP/MOS5SY) +ISOMOS	0.70	-	5.5

Digital Core Library Cells

X-FAB provides a standard cell library optimized for most typical applications in mixed signal ASIC. The 0.18-micron standard cells can be used for 0.18-micron four-metal, five-metal or six-metal tehnology including additionalprocess module options, e.g. 3.3V I/O module or 5.0V I/O module.

Name	Category	Density [1]	@ r_factor [3]	Main features
D_CELLS	standard	100 91 83	1.00 1.10 1.20	**high speed, more power consumption[4], more area[4], more noise[4]**
D_CELLSL	low power	118 [2] 107 98	1.00 1.10 1.20	**min area, min power consumption, less speed[5], less noise[5]**

1) library density: kGE/mm^2 at given routing factor (GE = NAND2 Gate Equivalent)
2) library cell density (utilization 100%)
3) r_factor = routing_factor
place&route_area =cell_area * routing_area
(averaged value: because routing factor, means wiring overhead, is netlist dependent)
Utilization [%] = 1/routing_factor * 100, e.g. r_factor = 1.20; utilization = 1/1.20 * 100 = 83%
4) more than low power library
5) less than standard library

Digital I/O Cells

The digital I/O libraries contain a comprehensive range of I/O cells divided into distinct inputs, outputs and bidirectionals.

The digital I/O library has the following features:

- Digital I/O library cells support the Low Power MOS or Standard MOS main process modules
- I/O cells are optimized for 3.3V or 5V IO operating voltage and 1.8V core operating voltage
- Pad limited I/O and core limited I/O variants
  - Pad-limited I/O cells require 4METALS and support also optionally 5METALS, 6METALS and THKMET technology modules
  - Core-limited I/O cells support 4METALS, 5METALS, 6METALS and THKMET technology modules
- The bond pad size is 53µm x 66µm
- The TTL and CMOS level detection circuits use low noise power rails
- Inputs and Bi-directional’s are available with gated input, pull-up, pull-down and hold options. Special inputs with Pi-type ESD protection structure can be used in applications where no P-type device to supply is allowed
- Outputs are available with selectable speeds to maintain low noise independent from DC output drive and can be configured as tri-state, bi-state, open drain or open source

Digital I/O Cells *(continued)*

		Pad Limited I/O Cells	Core Limited I/O Cells
Input		CMOS/TTL Level Schmitt Trigger Input	CMOS/TTL Level Schmitt Trigger Input
Input Option	Gated Pull-up	■	■
	Gated Pull-down	■	■
	Input Hold	■	■
	Gated CMOS Input	■	■
	Special Pi-type Inputs	■	■
	NAND Tree	■	■
Output		Tri-state Output or Open Orain Output	Tri-state Output or Open Drain Output
Output Drive		1, 2, 4, 8, 16, 24mA	1, 2, 4, 8, 16, 24mA
Slew Rate Control		■	■
Configurations		Bi-state Output Tri-state Output Open Drain Output Open Source Output	Bi-state Output Tri-state Output Open Drain Output Open Source Output
Cell Size	Cell Height	257µm	160µm
	Cell Width / Pad Pitch	60µm	84µm
ESD Robustness		4kV (HBM)	2kV (HBM)

RF CMOS I/O Pad Libraries

RFCMOS I/O pad cells are available for 3.3V or 5V operating voltage as RFPADS_3V or RFPADS_5V for triple metal Low Power MOS or Standard MOS main process modules. The RFPADS_3V and RFPADS_5V support also 4METALS, 5METALS and 6METALS technology modules. Special RFPADS_3VL and RFPADS_5VL RF CMOS I/O pad libraries are intended for use with the Thick Metal module and support also combinations with 4METALS and 5METALS technology modules.

The RFCMOS I/O pad libraries have the following features:

- RFCMOS I/O pad cells support Low Power MOS and Standard MOS main process modules
- Inalog RFCMOS I/O cells are available in variants with different ESD protection structures providing higher ESD level or lower pad capacitance as well as different series resistances
- All RFCMOS pad cells have a cell height of 156µm, a cell width of 96µm and use a 66µm x 66µm RF bond pad

Analog and RF Primitive Devices and Models

A very wide range of different analog primitives enable analog designers to develop sophisticated, high precision and reliable analog circuits.

High performance process modules, well-defined primitives devices and accurate device models are the key success factors for analog, RF and mixedsignal design. Combined with X-FAB's EDA support kit "TheKit" and state of the art design methodologies, first right mixed-signal designs can be realised.

X-FAB supports the latest BSIM3v3 models as the present SPICE model standard for MOS transistors. Bipolar transistors are modeled using the Gummel-Poon model for a given emitter size. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence. These resistances have to be simulated with the 3-terminal SPICE JFET model. High frequency MOS are modeled with three-terminal subcircuit including parasitic resistors, capacitors and diodes. The varactor is modeled as a two terminal voltage dependent capacitor subcircuit.

Model sets for most popular analog simulators, e.g. Spectre, HSPICE and ELDO are provided. The same characterization and modeling effort is spent for parasitic devices and 3rd order parameters, which are usually very important for analog design.

The matching behavior of MOS transistors, bipolar transistors, resistors and capacitors is investigated and characterized. Final matching parameters are extracted for all active and most of passive elements.

Analog Library Cells

Many analog and mixed-signal design projects are started in technologies with larger feature sizes because designers want to re-use existing analog cells. For easy migration to X-FAB's high performance XC018 process an increasing number of general purpose analog cells will be provided.

Examples for measured and modeled parameter characteristics

CMOS and Bipolar transistor Output Characteristics

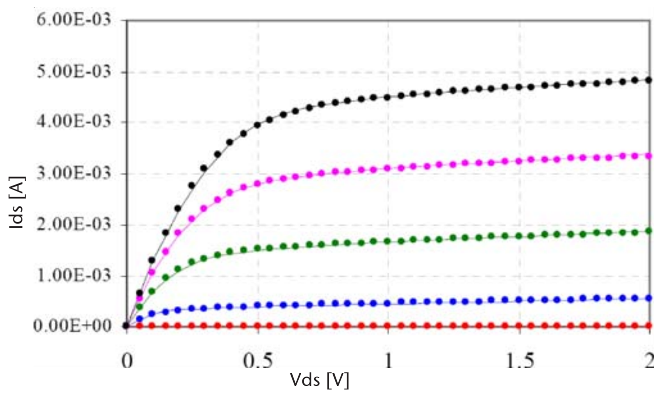


Figure 4: Device ne (MOSLP): Output characteristic for a typical wafer. W/L = 10/0.18, VGS = 0.6, 0.9, 1.2, 1.5, 1.8V VSB = 0V, Symbol = measured, line = BSIM3v3 model

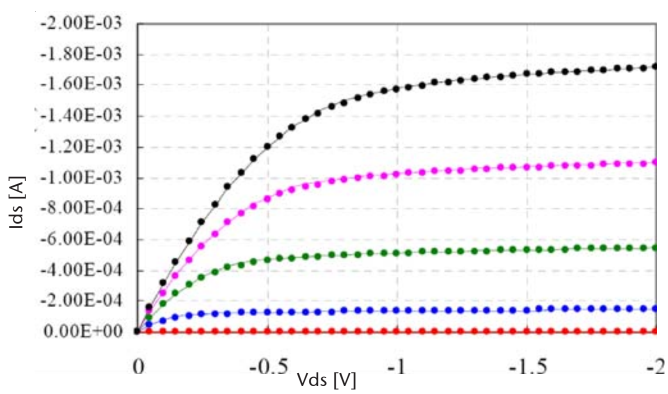


Figure 5: Device pe (MOSLP): Output characteristic for a typical wafer. W/L = 10/0.18, -VGS = 0.6, 0.9, 1.2, 1.5, 1.8V VSB = 0V, Symbol = measured, line = BSIM3v3 model

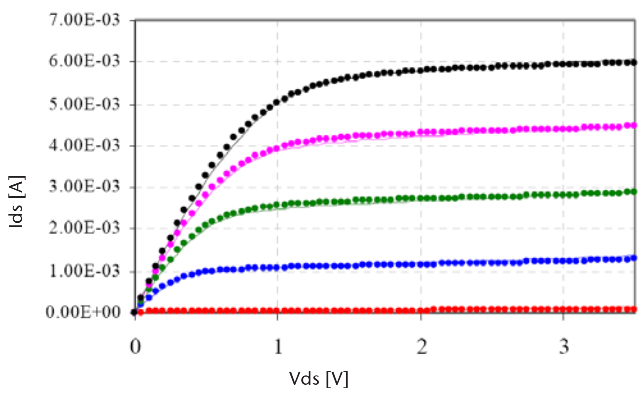


Figure 6: Device ne3 (MOS3ST): Output characteristic for a typical wafer. W/L = 10/0.35, VGS = 0.9, 1.5, 2.1, 2.7, 3.3V VSB = 0V, Symbol = measured, line = BSIM3v3 model

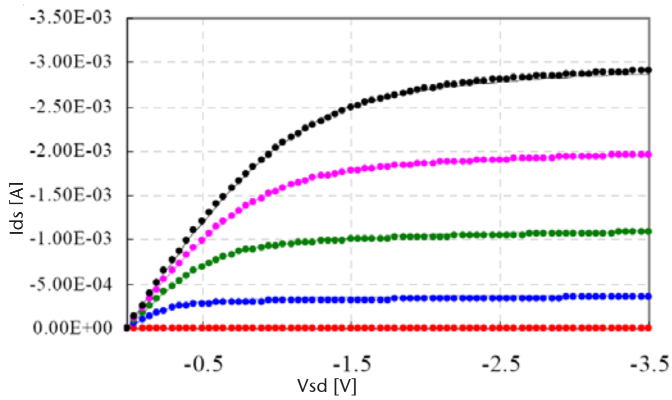


Figure 7: Device pe3 (MOS3ST): Output characteristic for a typical wafer. W/L = 10/0.30, -VGS = 0.9, 1.5, 2.1, 2.7, 3.3V VSB = 0V, Symbol = measured, line = BSIM3v3 model

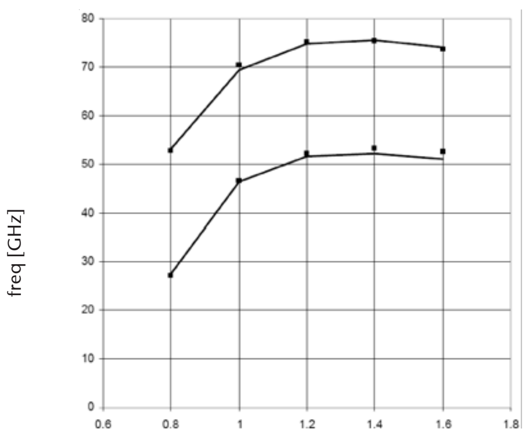


Figure 10: Device nerf: fT and fmax for a typical wafer. W/L = 5/0.18, ng = 6 VDS= 1.5V, Symbol = measured, line = BSIM3v3 model

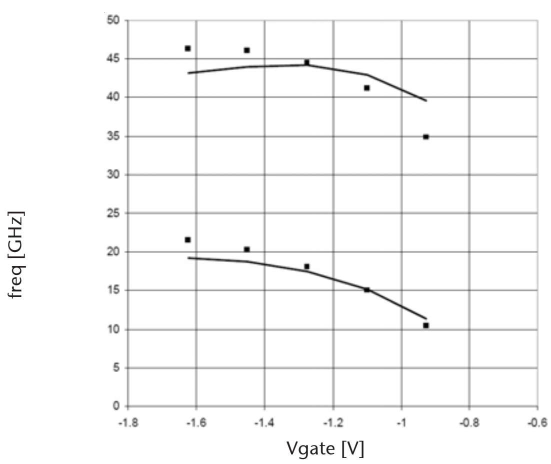


Figure 11: Device perf: fT and fmax for a typical wafer. W/L = 5/0.18, ng = 6 -VDS =1.5V, Symbol = measured, line = BSIM3v3 model

Examples for measured and modeled parameter characteristics *(continued)*

CMOS and Bipolar transistor Output Characteristics *(continued)*

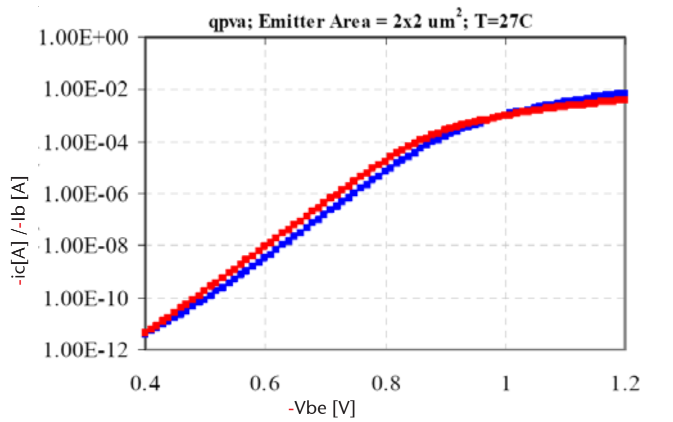


Figure 16: Device qpva (MOSST): Gummel plot of 1.8V vertical PNP bipolar transistor for a typical wafer. Vbc = 0.00V Symbol = measured, line = SPICE model

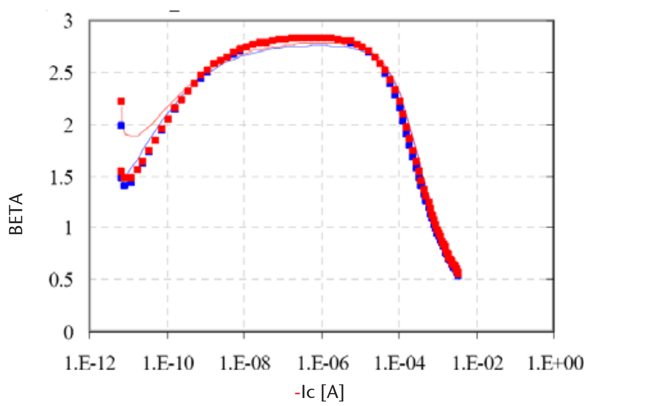


Figure 17: Device qpva (MOSST): Curren gain of 1.8V vertical PNP bipolar transistor for a typical wafer. -Vce = 0.9, 1.8V Symbol = measured, line = SPICE model

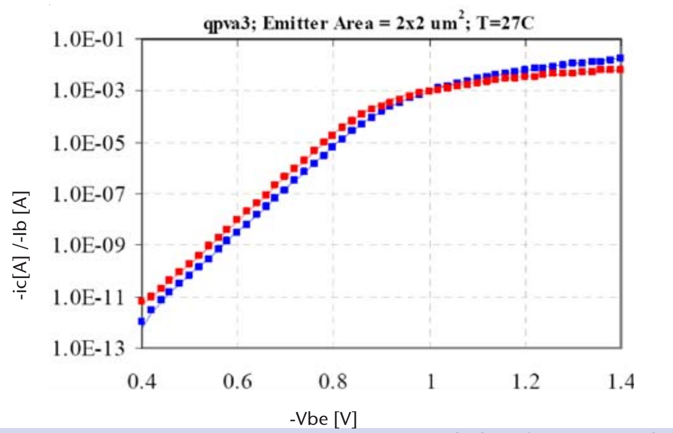


Figure 18: Device qpva3 (MOS3LP): Gummel plot of 3.3V vertical PNP bipolar transistor for a typical wafer. Vbc = 0.00V Symbol = measured, line = SPICE model

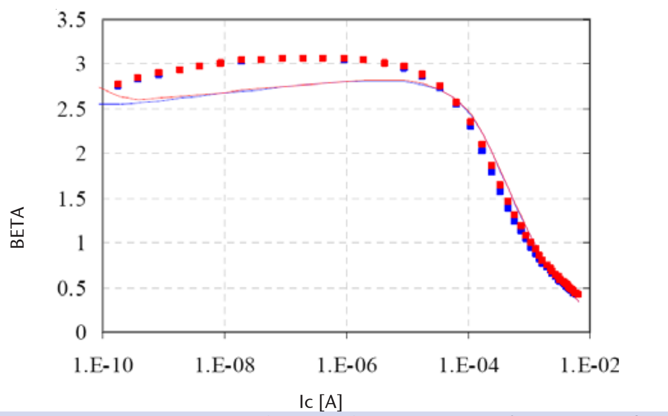


Figure 19: Device qpva3 (MOS3LP): Curren gain of 3.3V vertical PNP bipolar transistor for a typical wafer. -Vce = 1.65, 3.30V, Symbol = measured, line = SPICE model

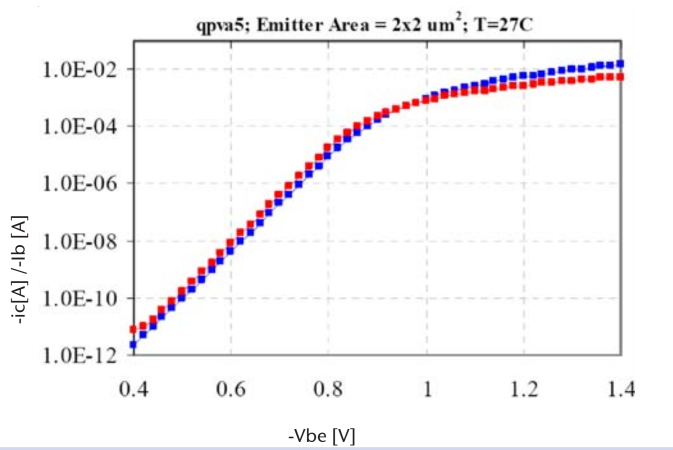


Figure 20: Device qpva5 (MOS5LP): Gummel plot of 5.0V vertical PNP bipolar transistor for a typical wafer. Vbc = 0.00V Symbol = measured, line = SPICE model

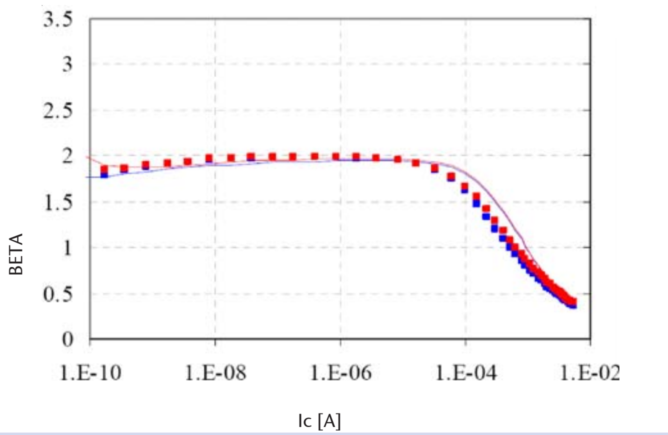


Figure 21: Device qpva5 (MOSLP): Curren gain of 5.0V vertical PNP bipolar transistor for a typical wafer. -Vce = 1.65, 5.0V Symbol = measured, line = SPICE model

Examples for measured and modeled parameter characteristics *(continued)*

Inductor and Varactor Output Characteristics

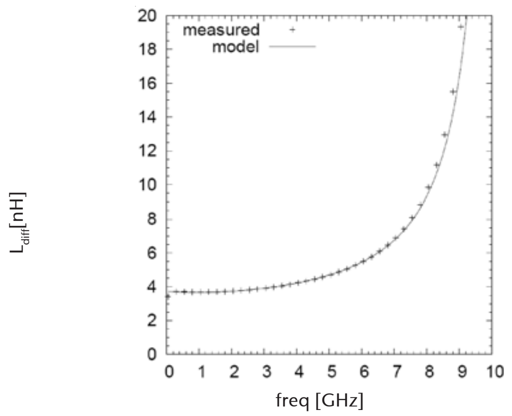


Figure 22: Device I24a: Inductance of symmetrical 3.8nH inductor for 2.4GHz for a typical wafer.
Symbol = measured, line = SPICE model

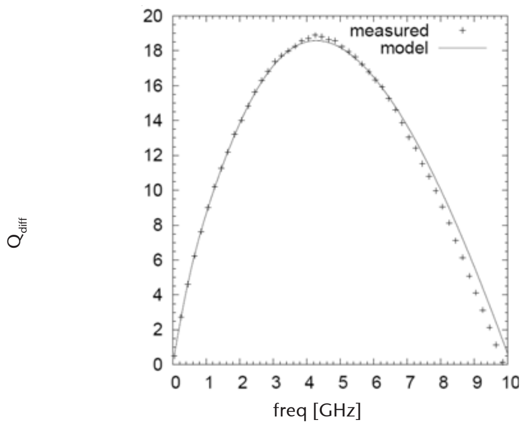


Figure 23: Device I24a: Quality factor of symmetrical 3.8nH inductor for 2.4GHz for a typical wafer.
Symbol = measured, line = SPICE model

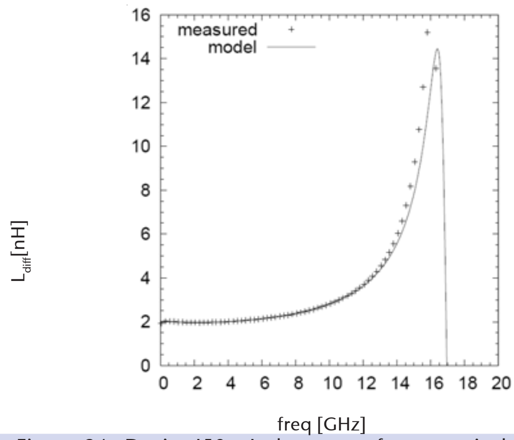


Figure 24: Device I50a: Inductance of symmetrical 2.0nH inductor for 5.0GHz for a typical wafer.
Symbol = measured, line = SPICE model

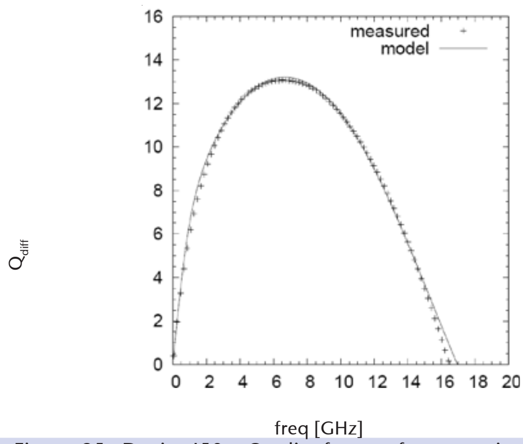


Figure 25: Device I50a: Quality factor of symmetrical 2.0nH inductor for 5.0GHz for a typical wafer.
Symbol = measured, line = SPICE model

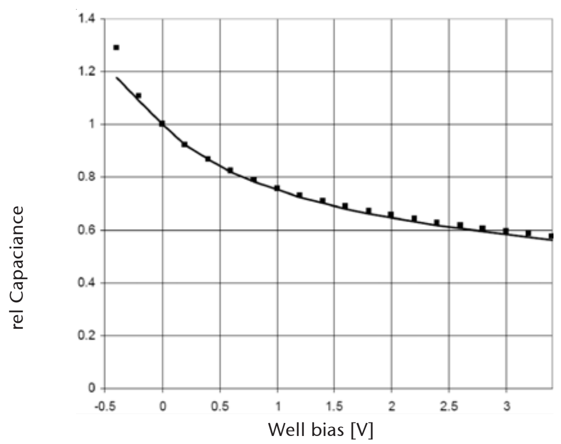


Figure 26: Device dpvc: Capacitance vs voltage of 1.8V diode varactor for a typical wafer.
Symbol = measured, line = SPICE model

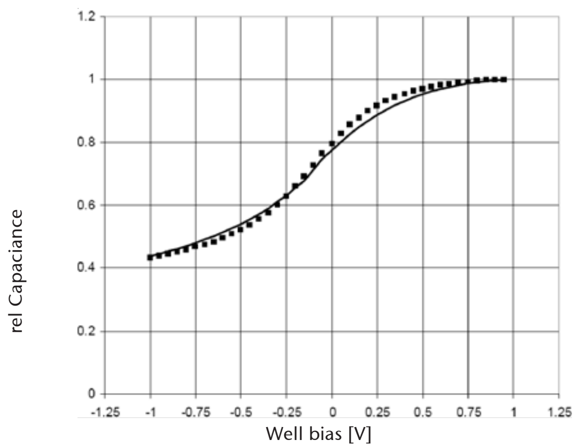
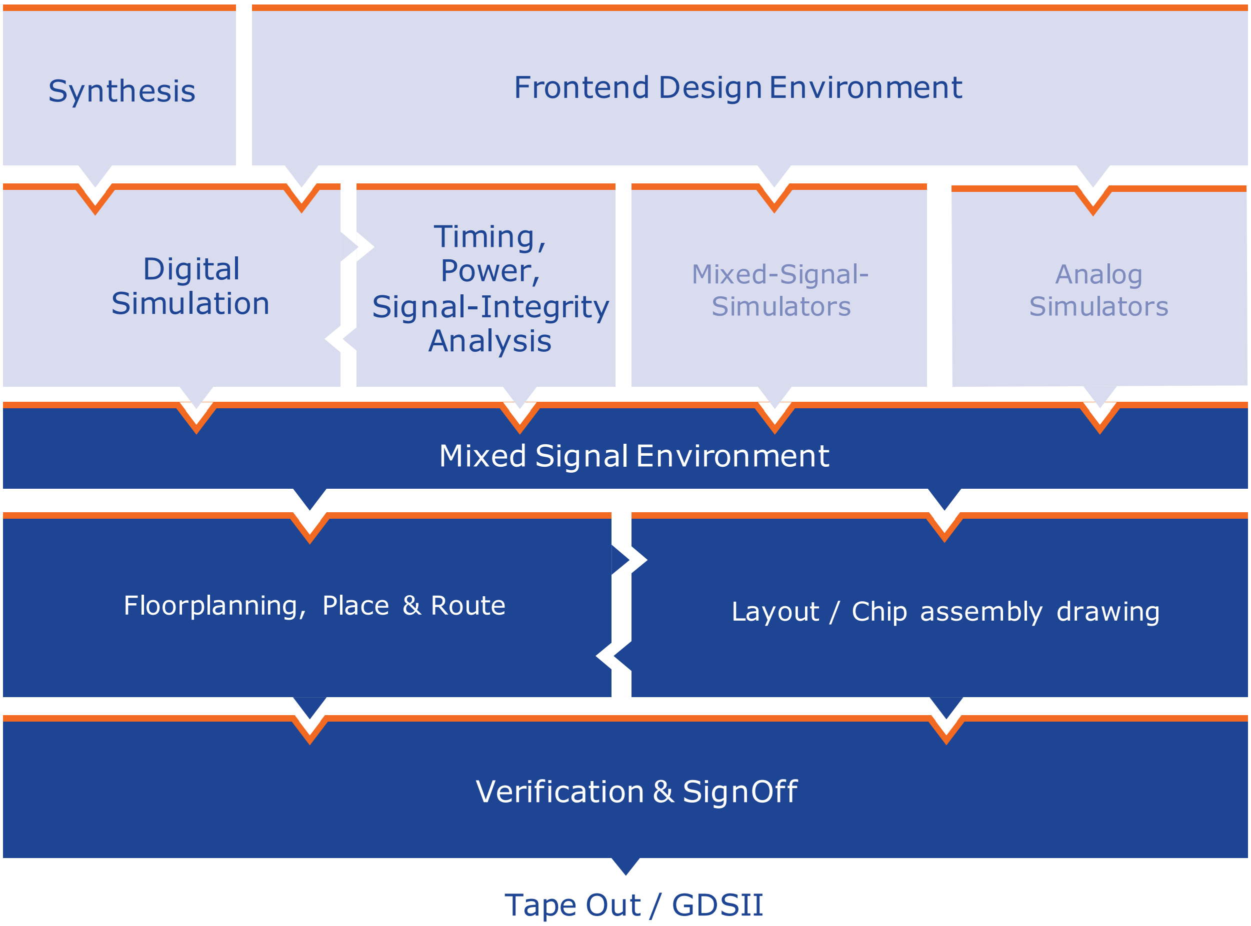


Figure 27: Device mosvc: Capacitance vs voltage of 1.8V MOS varactor for a typical wafer.
Symbol = measured, line = SPICE model

Supported EDA Tools



Note: Diagram shows overview of all X-FAB supported EDA tools. For XC018, registered customers get more details on X-TIC.

X-FAB's IC Development Kit "TheKit"

The X-FAB IC Development **Kit** is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. It comes with documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits.

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