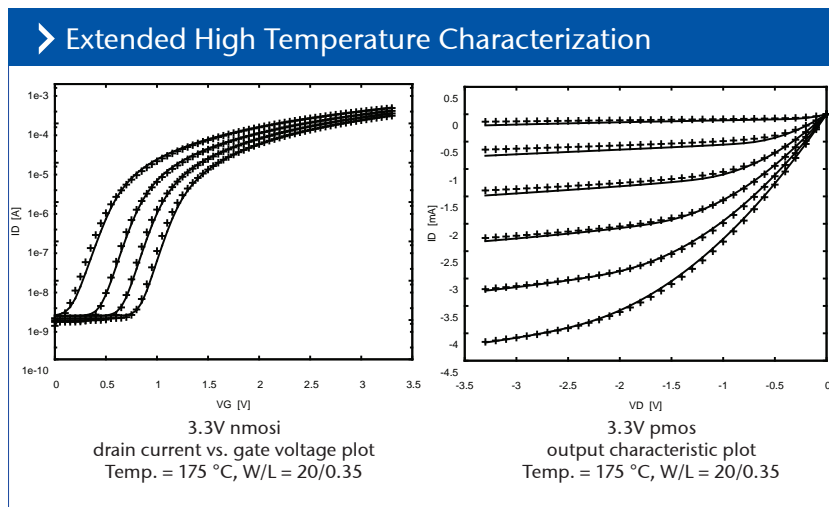
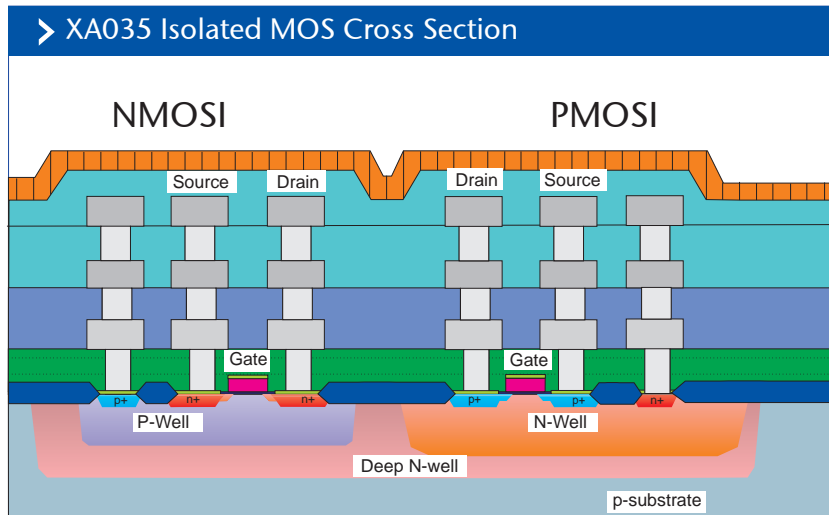


## > XA035

### High Temperature combining HV and NVM modular CMOS Technology

> Modular 0.35  $\mu\text{m}$  High Temperature CMOS process with operating temperature up to 175  $^{\circ}\text{C}$ .

The XA035 process is ideally suited for high-precision analog circuits, sensor front-ends, and brushless DC motor controls for automotive, industrial, aerospace and military markets.



#### > Module Overview

CORE

CORE

3.3V MOS module, 1P3M

FEOL

ISOMOS

Isolated MOS module

THKOX

Thick gate oxide module

DEPL

Depletion NMOS module

BURDIF

Buried N module

CAPPOLY

Polysilicon 2 module

HRPOLY

High resistance polysilicon 1 module

XRPOLY

Very high resistance polysilicon 1 module

TEEPROM

EEPROM module

BEOL

MIM

MIM capacitor module

DMIM

Double MIM module

METAL2

Top metal 2 module

METAL4

Metal 4 module

THKMET

Thick metal 4 module

# 0.35 μm CMOS Process Family

## > XA035

### Features

- 3.3V logic layout & performance compatible with industry standard
- Extended high temperature characterisation, up to 175 °C operating temperature
- Device model improvement, accurate device matching for high temperature environment
- Level 1 lifetime specification in Process Reliability document
- Lifetime calculator tool for device reliability estimation based on automotive mission profile
- High-voltage component up to 45V and 14V automotive board net ready
- NVM with EEPROM and OTP option (Zener Zap)
- RF characterisation and models for all RF MOS transistors and passive components
- High density RAM, DPRAM and ROM blocks
- Diva, Dracula, Calibre DRC & LVS parasitic extraction

### Capacitors (Selection)

Parameter	Area Cap [fF/μm <sup>2</sup> ]	BV [V]	Max VTB [V]
poly1/poly2 cap.	0.85	30	45
POD cap.	3.90	8.6	18
MIM cap.	1.25	30.2	45
DMIM cap.	2.5	30	45

### Resistors (Selection)

Parameter	RS [Ω/□]	Temp. Coeff [10 <sup>-3</sup> /K]	Max VTB [V]
Low TC poly2 resistor	200	-0.7	45
N+ high res. poly resistor	1000	-2.8	45
Very high res. poly resistor	10000	-4.3	45

### Bipolar Transistors (Selection)

Parameter	BETA	VA [V]	Max VCE [V]
Vertical PNP	4.5	190	3.6
Lateral PNP	27	4.2	3.6
Isolated vertical NPN	48	38	5.5



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### Design Rules

Parameter	Min. Width [μm]	Min. Spacing [μm]
N-well	1.6	1.0
Active Area	0.5	0.6
Polysilicon Gate	0.35	0.45
Contact	0.4	0.4
Metal 1/ 2	0.5	0.45/0.5
Via 1/ 2/ 3	0.5	0.45
Metal 3 (Top M)	0.5	0.6
Metal 4	0.6	0.6
Thick Metal 4	3.0	2.5

### MOS Transistors (Selection)

Parameter	VT  [V]	RDSon [kΩ.μm]	BVDSS [V]	Max VGS [V]
3.3V NMOS	0.60	-	>5.5	3.6
3.3V PMOS	0.74	-	>5.5	3.6
5V NMOS	1.15	-	12	5.5
5V PMOS	0.95	-	9.6	5.5
12V NMOS	0.59	17	15	3.6
14V drain & source NMOS	1.00	11	>20	18
14V drain & source PMOS	0.95	30	>20	18
18V drain & source NMOS	1.00	15	>20	18
18V drain & source PMOS	1.00	40	>20	18
45V drain depletion NMOS	1.2	14	58	18
45V N-DMOS (thick oxide)	1.40	19.5	70	18
45V N-DMOS (thin oxide)	0.55	20	70	3.6

### Diodes (Selection)

Parameter	Vf [V]	Vr @ 100nA [V]	BVr [V]
Polysilicon diode	1.2	4.7	6.8

### EEPROM

Parameter	Values
Supply voltage	1.8V ... 3.6V
Configuration	up to 16Kbit including charge pump
Temperature range	-40 ... +175 °C (read) / +125 °C (write)
Data retention	10 years @ 85 °C

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