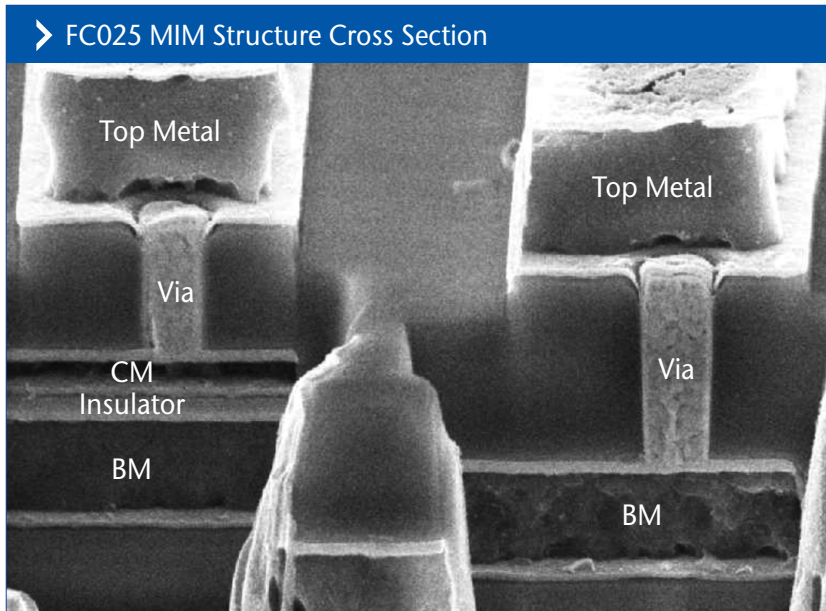
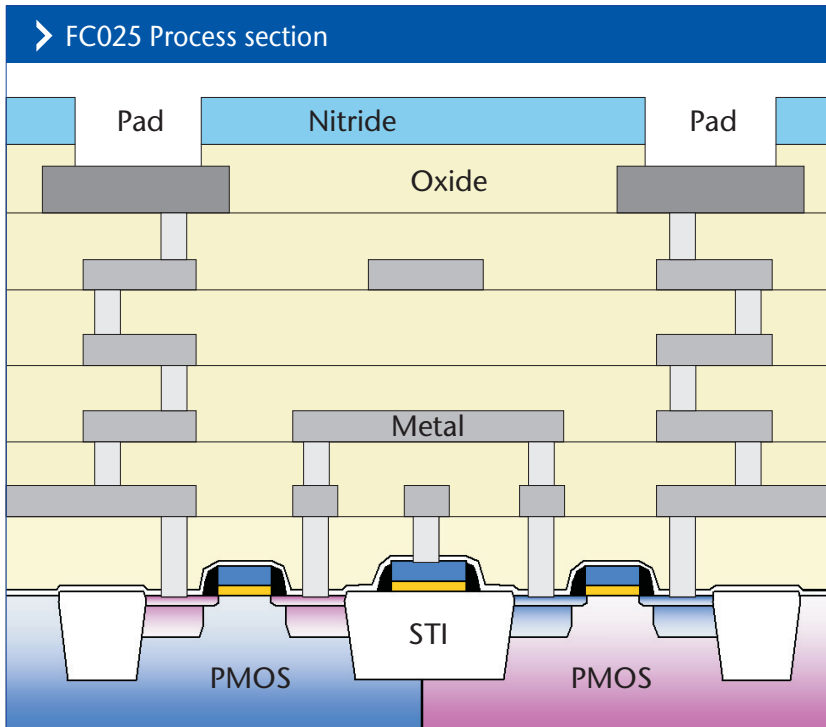


0.25 μm CMOS Process Family



> FC025

> 0.25 μm CMOS process for 2.5V logic and mixed-signal applications with 3.3V or 5V I/O



> Main Process Features

- Single Poly and up to 5 Metal Layers
 - Well Architecture: Retrograde Twin Well
 - Isolation: Shallow Trench Isolation
 - Gate Oxide: 2.5V 50Å
3.3V 70Å^[1]
5.0V 130Å^[2]
 - Gate Poly: Ti Salicide with Block option
 - ILD Planarization: BPSG and CMP
 - IMD Planarization: HDP and CMP
 - Contact & Via: W-Plug with W-CMP
 - Metal Scheme: AlCu
- [1] 2.5V with 3.3V option
[2] 2.5V with 5V option

> Value Added Option

- Embedded Flash: 2P3M SST SuperFlash® x8 and x16 macros
- 6T SRAM cell: 7.56 μm^2 & 10.95 μm^2
- Ring Oscillator: 43ps/stage

0.25 μm CMOS Process Family

> FC025

2.5V/3.3V logic and mixed-signal variants

- Logic layout & performance compatible with the industry standard
- Standard cell library, up to 70k gates/mm²
- 3.3V / 5V tolerant I/O's
- 5.0V transistors (dual gate) optional
- High value polysilicon resistor optional
- Fully documented and characterized
- BSIM3v3.1 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterized & included in model
- Calibrated interconnect model
- Diva, Dracula, Hercules & Calibre DRC & LVS verification decks
- Calibre-xRC & Star-RCXT LPE verification decks
- Cadence PDK

Resistors	
Resistors Device	Sheet Resistance [Ω/□]
N+ Poly resistor (salicide)	5
P+ Poly resistor (salicide)	5
N+ Poly resistor	190
P+ Poly resistor	160
P+ Poly resistor high	900
P+ diffusion salicided resistor	4.0
P+ diffusion resistor	140
N+ diffusion salicided resistor	4.5
N+ diffusion resistor	65
N-well resistor	1100
Metal 1	0.08
Metal 2 or 3 or 4	0.06
Metal 5 (top metal)	0.04

Capacitors		
Device	Area Cap [fF/μm ²]	BV [V]
Poly1 - Poly2	0.9	>10
Metal-insulator-Metal	1.0	>10

IP/Libraries	
IP/Libraries	Vendor
Standard Cell Libraries	ARM
I/O Pad Libraries	ARM
Diffusion ROM Compiler	ARM
SP & DP SRAM Compiler	ARM
2P Register File Compiler	ARM
USB 1.1 I/O	ARM
PLL Compiler	Ceva
LDO Voltage regulator	ICDS
Power On Reset	ICDS
Bandgap	ICDS
Video DAC	ICDS
DC – DC Converter	ICDS

Design Rules	
Parameter	Size [μm]
N-well width	1.2
Active area width	0.3
Polysilicon gate	0.24
Contact width	0.3
Metal 1 width	0.32
Via 1 or 2 or 3 or 4 width	0.36
Metal 2 or 3 or 4 width	0.4
Metal 5 width	0.44

Transistors Parameters			
Device	V _t [V]	I _{DS} [μA/μm]	BVDSS [V]
NMOS 2.5V	0.53	600	> 5
PMOS 2.5V	-0.53	-270	< -5
NMOS 3.3V	0.53	580	> 6
PMOS 3.3V	-0.83	-230	< -6
NMOS 5.0V	0.83	530	> 7
PMOS 5.0V	-0.82	-240	< -7

EFLASH Macros
Macro Size
16K x8, 32K x8, 64K x8, 128K x8
32K x16, 128K x16, 256K x16



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