

# 0.25 $\mu\text{m}$ CMOS Process

## > FC025

### 0.25 Micron CMOS Technology

<b>&gt; Description</b>	The FC025 series is X-FAB's 0.25-micron Modular Logic and Mixed Signal Technology. Main target applications are standard cell, semi-custom and full custom designs for consumer and communication products. Based upon an industry stan-	dard single poly with up to five metal layers 0.25-micron drawn gate length N-well process, modules are available for five layers of metal, double poly/metal capacitors, high resistive poly and dual gate oxide (5V) transistors.
<b>&gt; Key Features</b>	<ul style="list-style-type: none"><li>- 2.5V Logic Layout &amp; performance compatible with the industry standard</li><li>- 0.25-micron single poly, up to five metal N-well CMOS basic process</li><li>- Five layer metal options for high density circuits</li><li>- Double Poly/Metal Capacitor</li><li>- Salicided source &amp; drain</li><li>- Direct STI</li><li>- Deep N-well module</li><li>- 2.5V Core, 3.3V/5V tolerant I/O</li><li>- 5 V Module optional</li><li>- Gate oxide thickness: 5.0V - 130Å, 3.3V - 70Å, 2.5V - 50Å</li><li>- Typical and worst-case models - BSIM3v3.1 (MOS, BJT, RES, CAP)</li><li>- MOS 1/f noise characterized &amp; included in model</li><li>- Diva, Dracula, Hercules &amp; Calibre DRC &amp; LVS verification decks</li><li>- Calibre-xRC &amp; Star-RXCT LPE verification decks</li></ul>	
<b>&gt; Applications</b>	<ul style="list-style-type: none"><li>- Standard Logic/controller circuits</li><li>- Mixed signal embedded systems/ systems on a chip (SOC)</li><li>- Low power mixed signal circuits</li><li>- Embedded Flash</li><li>- CMOS Sensor controller</li><li>- Communications, consumer and industrial markets</li></ul>	
<b>&gt; Quality Assurance</b>	X-FAB spends a lot of possible effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by strict quality improvement	procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, ISO TS 16 949*, BS7799 and other standards.  * Received letter of conformance
<b>&gt; Deliverables</b>	<ul style="list-style-type: none"><li>- PCM tested wafers</li><li>- Optional production services: wafer sort, assembly and final test</li><li>- Optional Engineering services: Multi Project Wafer (MPW), Prototyping tape-outs</li><li>- Optional Design services; e.g. feasibility studies, place &amp; route, synthesis, custom block development</li></ul>	
<b>&gt; Digital Libraries</b>	<ul style="list-style-type: none"><li>- Foundry-specific optimized libraries</li><li>- Standard core library for high speed digital blocks</li><li>- SP/DP SRAM, 2P RF, Diffusion ROM compilers</li></ul>	
<b>&gt; Analog Libraries</b>	<ul style="list-style-type: none"><li>- Bandgaps</li><li>- Digital-To-Analog Converters</li><li>- RC Oscillators</li><li>- Power-On-Reset</li><li>- Video DAC</li></ul>	
<b>&gt; Primitive Devices</b>	<ul style="list-style-type: none"><li>- NMOS/PMOS Transistors (2.5V, 3.3V, 5.0V)</li><li>- Bipolar Transistors</li><li>- Diodes</li><li>- Capacitors</li><li>- Resistors</li></ul>	

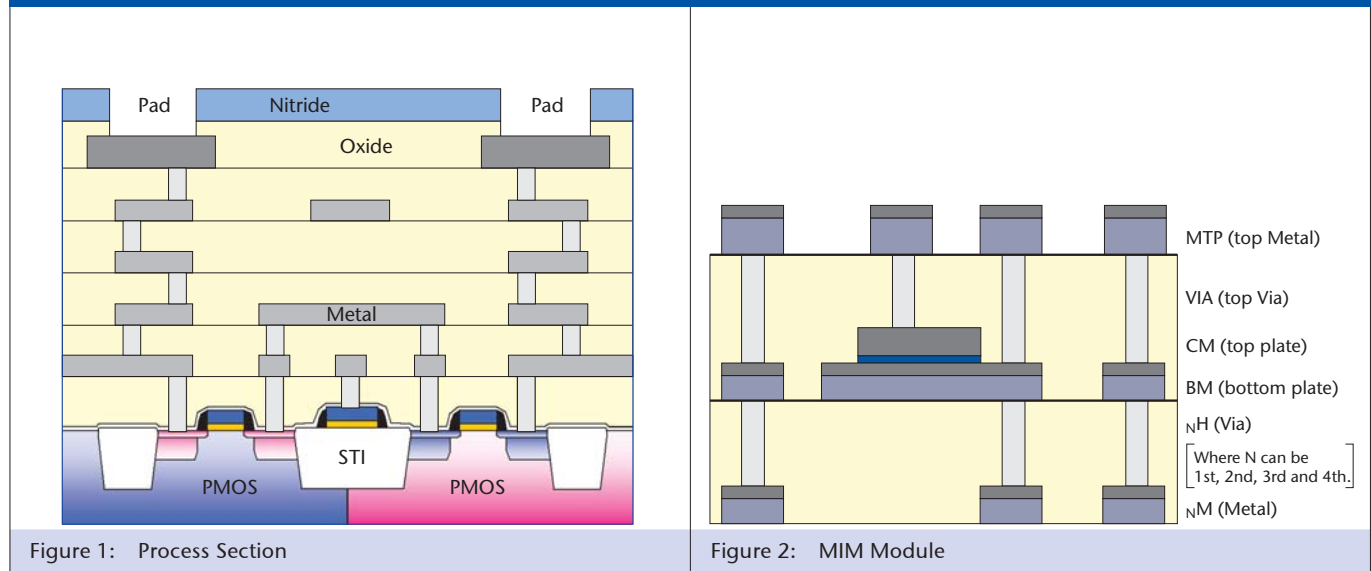
Process Options			
Module Name	Number of Masks	Remarks	Typical Primitive Devices Applications
CMOS Core (1P3M)	17	P-prime wafer, single poly, triple metal	2.5V/3.3V NMOS/PMOS, digital applications

To get the available technology options; this main module can be combined with one or more of the following additional modules:

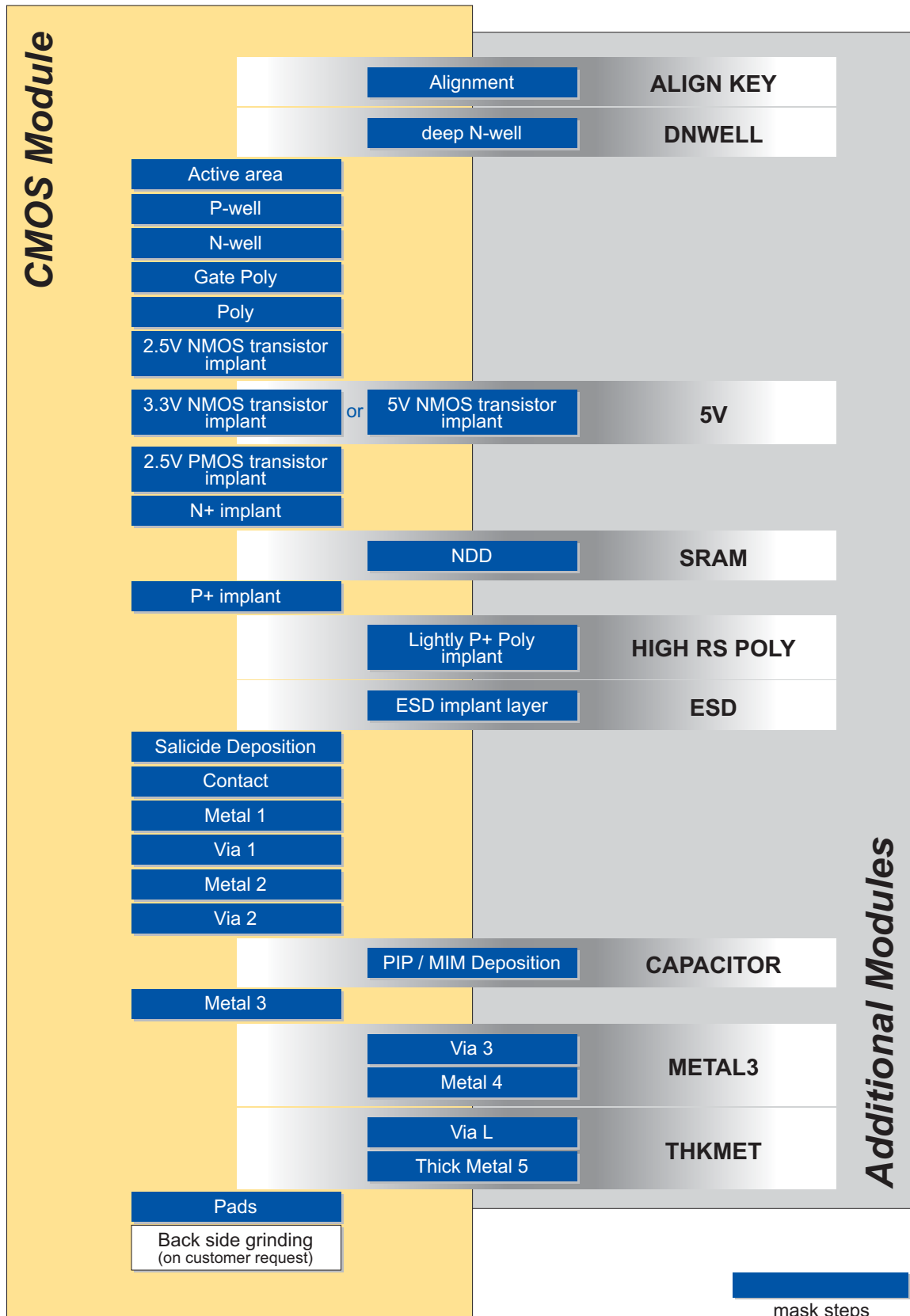
Module Name	Number of additional Masks	Remarks	Typical Primitive Devices Applications
PIP	2	Double polysilicon process	Capacitor
MIM	1	Metal-insulator-Metal process	Capacitor
HRPOLY	1	LPP mask	High value resistor
5 Volt	2	RACT & NW2 masks	5 Volt NMOS & 5 Volt PMOS transistors
Deep Nwell	2	Deep Nwell implantation	Noise isolation
SRAM	1	7.56µm <sup>2</sup> SRAM process	SRAM bit cell
Metal 4	2	Additional Metal layer	More complex wiring
Metal 5	2	Additional Metal layer	More complex wiring

Module Name	Number of Masks	Remarks	Typical Primitive Devices Applications
eFlash (2P3M)	32	P-prime wafer, double poly, logic with mixed signal, embedded Flash	2.5V/3.3V NMOS/PMOS, Smart card / MCU

> Schematic Cross Sections



> Main Process Flow



Basic Design Rules		
Mask	Width [μm]	Spacing [μm]
N-Well	1.2	2.0
Active Area	0.3	0.4
Poly-Silicon Gate	0.24	0.4
Contact	0.3	0.3
Metal 1	0.32	0.32
Via 1	0.36	0.35
Metal 2	0.4	0.4
Via 2	0.36	0.35
Metal 3	0.4	0.4
Via 3	0.36	0.35
Metal 4	0.4	0.4
VTP	0.36	0.35
MTP	0.44	0.46

> Device Parameters

**Active Devices** (typical data)

MOS Transistors				
Device	Available with module	VT  [V]	IDS [μA/μm]	BVDSS  [V]
NMOS 2.5V	core	0.53	600	> 5
PMOS 2.5V	core	-0.53	-270	< -5
NMOS 3.3V	3.3V I/O	0.53	580	> 6
PMOS 3.3V	3.3V I/O	-0.83	-230	< -6
NMOS 5V	5V I/O	0.83	530	> 7
PMOS 5V	5V I/O	0.82	-240	< -7

**Passive Devices** (typical data)

Capacitors			
Device	Area Cap [fF/μm <sup>2</sup> ]	BV [V]	Voltage coefficient [ppm/V]
Poly1-Poly2	0.9	>10	200
Metal-insulator-Metal	1.0	>10	100

> Device Parameters (continued)

Passive Devices (typical data) (continued)

Resistors & Conductors			
Device	RS [Ω/□]	Thickness [μm]	Max J/W [mA/μm]
N+ Poly resistor (salicide)	5	0.20	-
P+ Poly resistor (salicide)	5	0.20	-
N+ Poly resistor (non-salicide)	190	0.16	-
P+ Poly resistor (non-salicide)	160	0.16	-
P+ Poly resistor high Rs (non-salicide)	900	0.16	-
P+ Poly resistor medium Rs (non-salicide)	500	0.16	-
P+ diffusion silicided resistor	4.0	0.22	-
P+ diffusion resistor	140	0.17	-
N+ diffusion silicided resistor	4.5	0.20	-
N+ diffusion resistor	65	0.15	-
N-well resistor	1100	1.5	-
Deep N-well resistor	500	-	-
Metal 1	0.08	0.44	1
Metal 2	0.06	0.44	1
Metal 3	0.06	0.44	1
Metal 4	0.06	0.44	1
Metal 5 (top metal)	0.04	0.85	1.6

> Digital Core Library Cells

ARM Standard cells up to 70K gates/mm<sup>2</sup>  
 6T SRAM Cell: 7.56μm<sup>2</sup> & 10.95μm<sup>2</sup>

Memory Compilers:

- ARM – SP & DP SRAM Compiler
- ARM – 2P RF Compilers
- ARM – Diffusion ROM Compiler

eFlash Macro	
IP Macro	Configuration
AF16K8AF25	16K x 8
AF32K8AF25	32K x 8
AF32K8BF25	32K x 8
AF64K8AF25	64K x 8
AF64K8BF25	64K x 8
AF128K8GF25	128K x 8
AF256K8CF25	256K x 8
AF256K16FF25	256K x 16

> Digital I/O Cells

The digital I/O library contains a comprehensive range of I/O cells divided into distinct inputs, outputs and bidirectionals with variants for single voltage and dual voltage devices.

The digital I/O library has the following features:

- ARM – Integral I/O (90um pitch)
- ARM – GPIO (60um pitch)
- ARM – USB 1.1 IO
- ARM – 5V tolerant I/O cells are available.

> Logic & Mixed Signal Primitive Devices and Models

See section “Device Parameters” for details.  
 X-FAB’s CAE support kit Cadence PDK.  
 X-FAB supports BSIM3 models as the present SPICE model standard for MOS transistors. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence. These resistances have to be simulated with the 3-terminal SPICE JFET model.  
 Model sets for most popular analog simulators, e.g. Spectre, HSPICE and PSPICE are provided.

> Examples for measured and modeled parameter characteristics

CMOS and Bipolar Transistor Output Characteristics

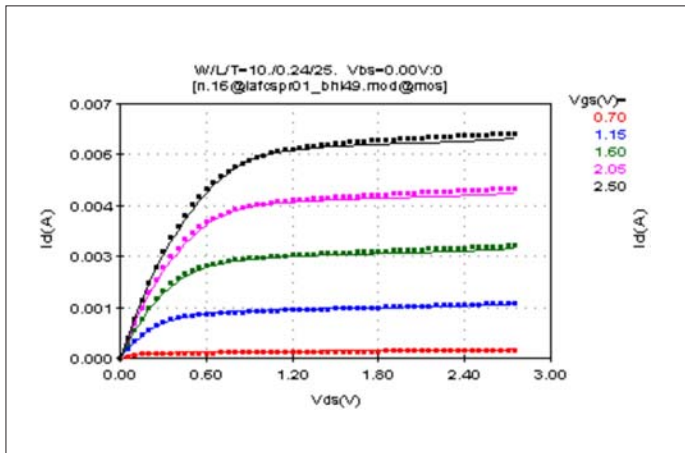


Figure 3: 2.5V NMOS Output Characteristic

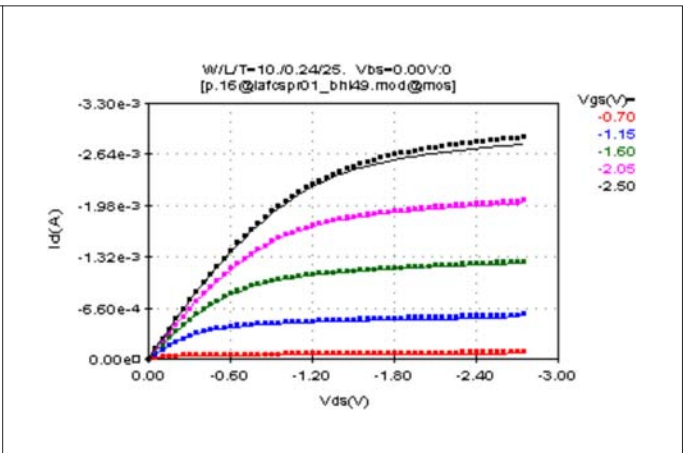


Figure 3: 2.5V PMOS Output Characteristic

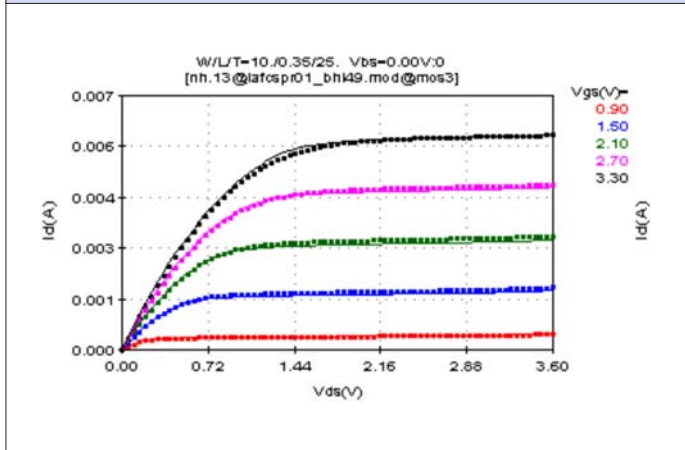


Figure 5: 3.3V NMOS Output Characteristic

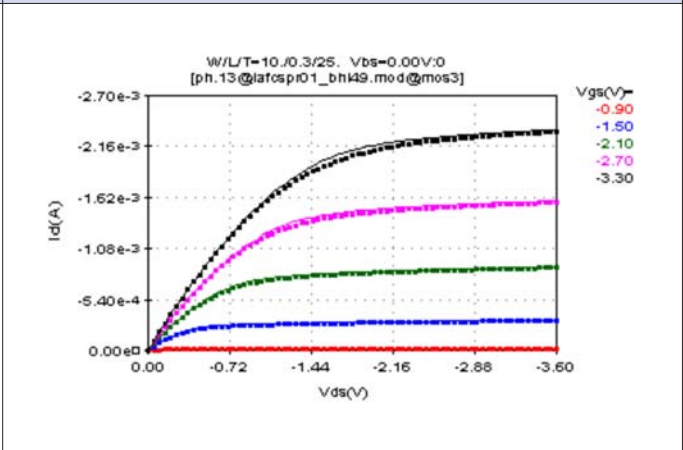


Figure 6: 3.3V PMOS Output Characteristic

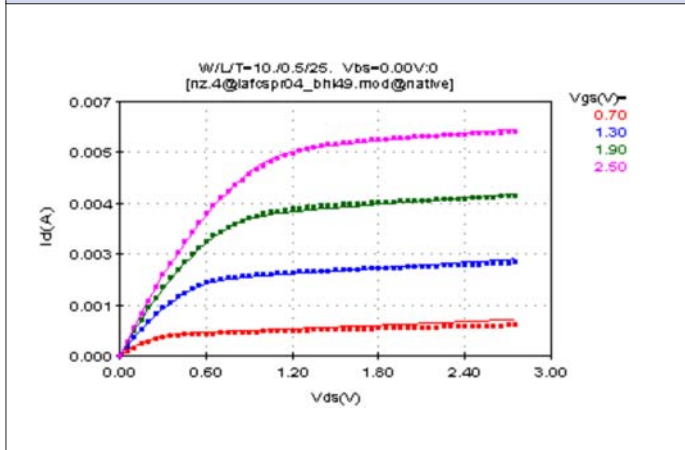


Figure 7: 2.5V Native NMOS

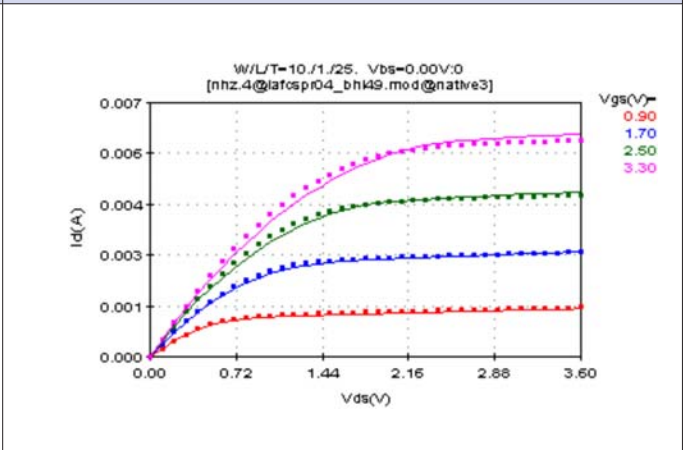


Figure 8: 3.3V Native NMOS

> Examples for measured and modeled parameter characteristics (continued)

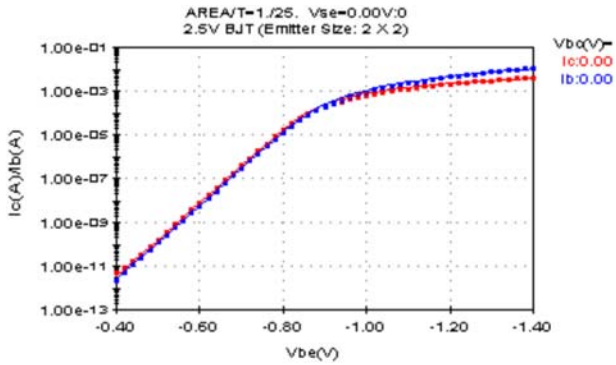


Figure 9: 2.5V BJT (Emitter size 2x2 μm<sup>2</sup>) Gummel Plot

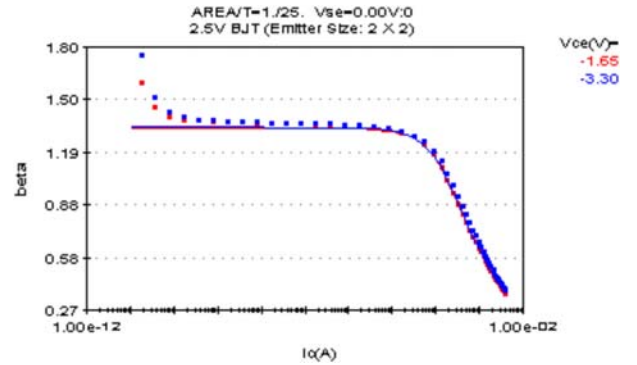


Figure 10: Gain vs collector current

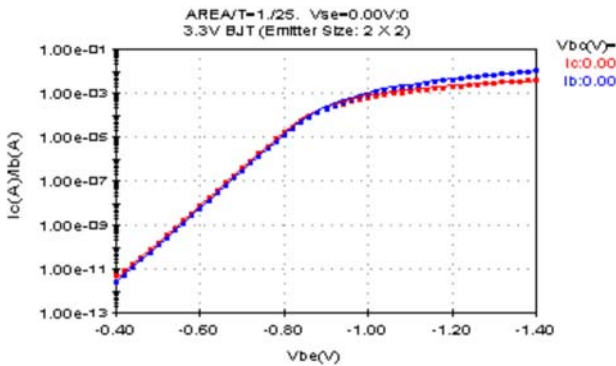


Figure 11: 3.3V BJT (Emitter size 2x2 μm<sup>2</sup>) Gummel Plot

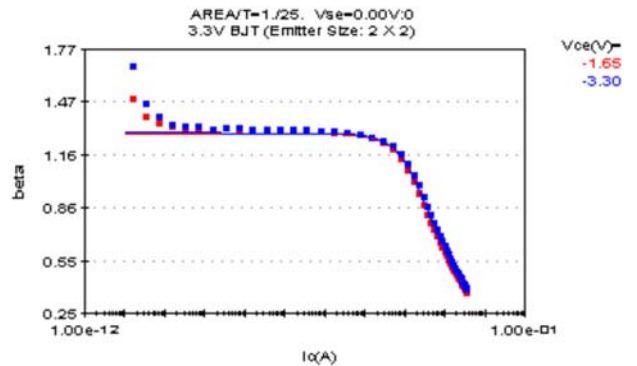


Figure 12: Gain vs collector current

Matching

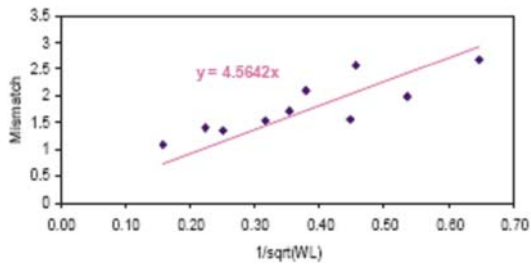


Figure 13: 2.5V NMOS Vt Matching

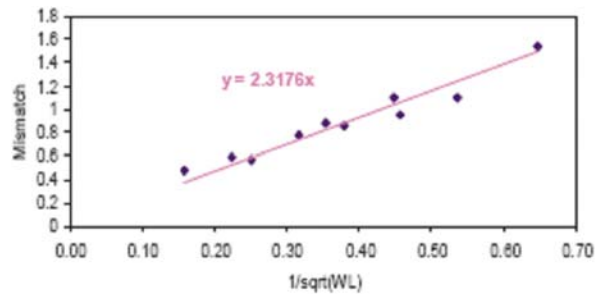


Figure 14: 2.5V PMOS Vt Matching

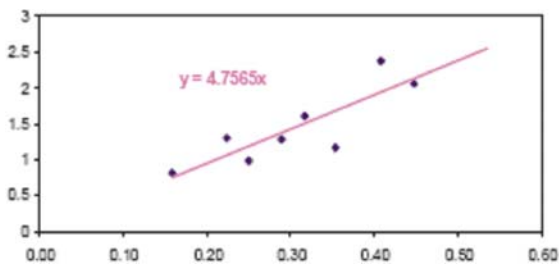


Figure 15: 3.3V NMOS Vt Matching

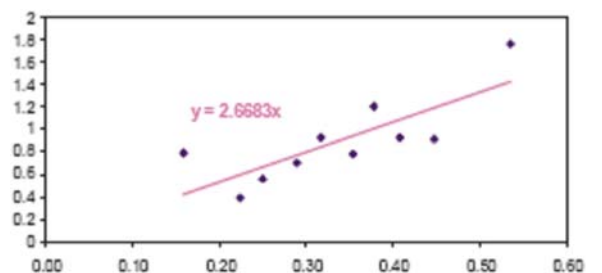


Figure 16: 3.3V PMOS Vt Matching

> Examples for measured and modeled parameter characteristics (continued)

Resistor Matching

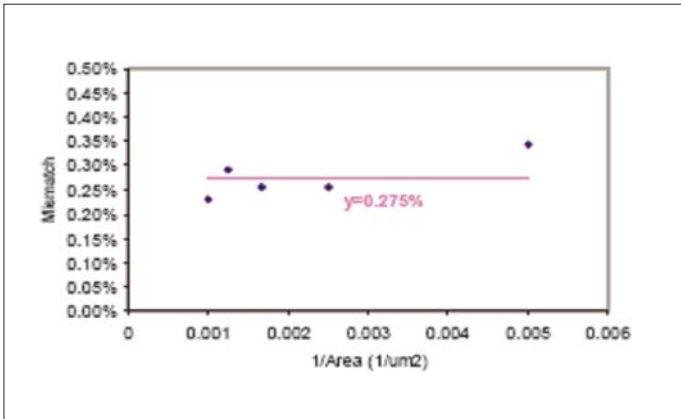


Figure 17: N+ Poly Resistance Matching

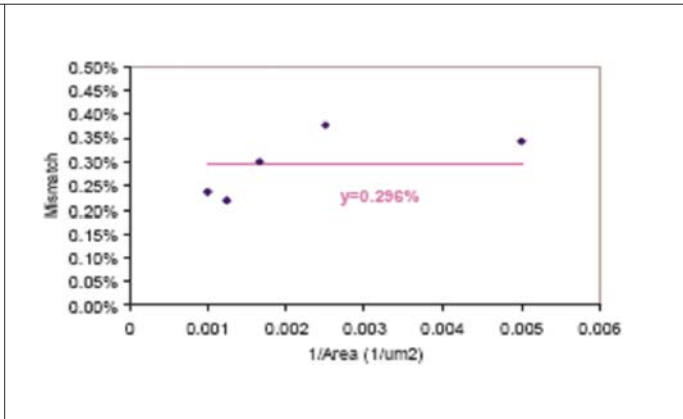


Figure 18: P+ Poly Resistance Matching

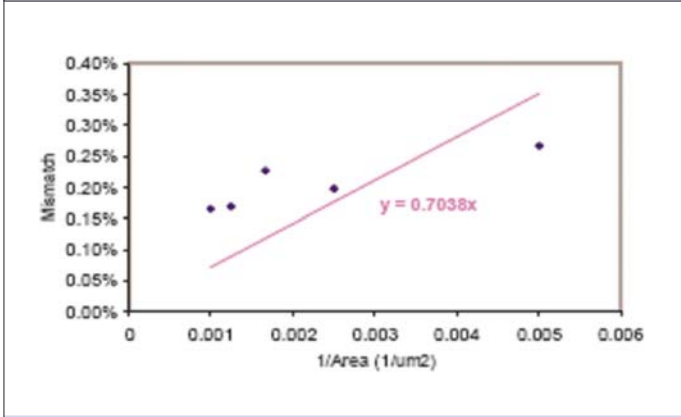


Figure 19: N+ Poly (non-salicide) Resistance Matching

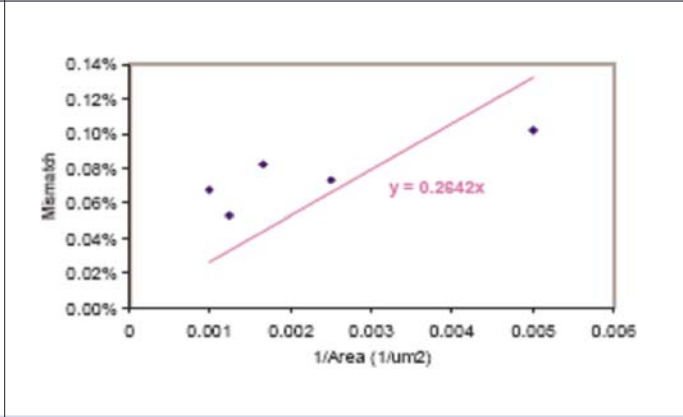
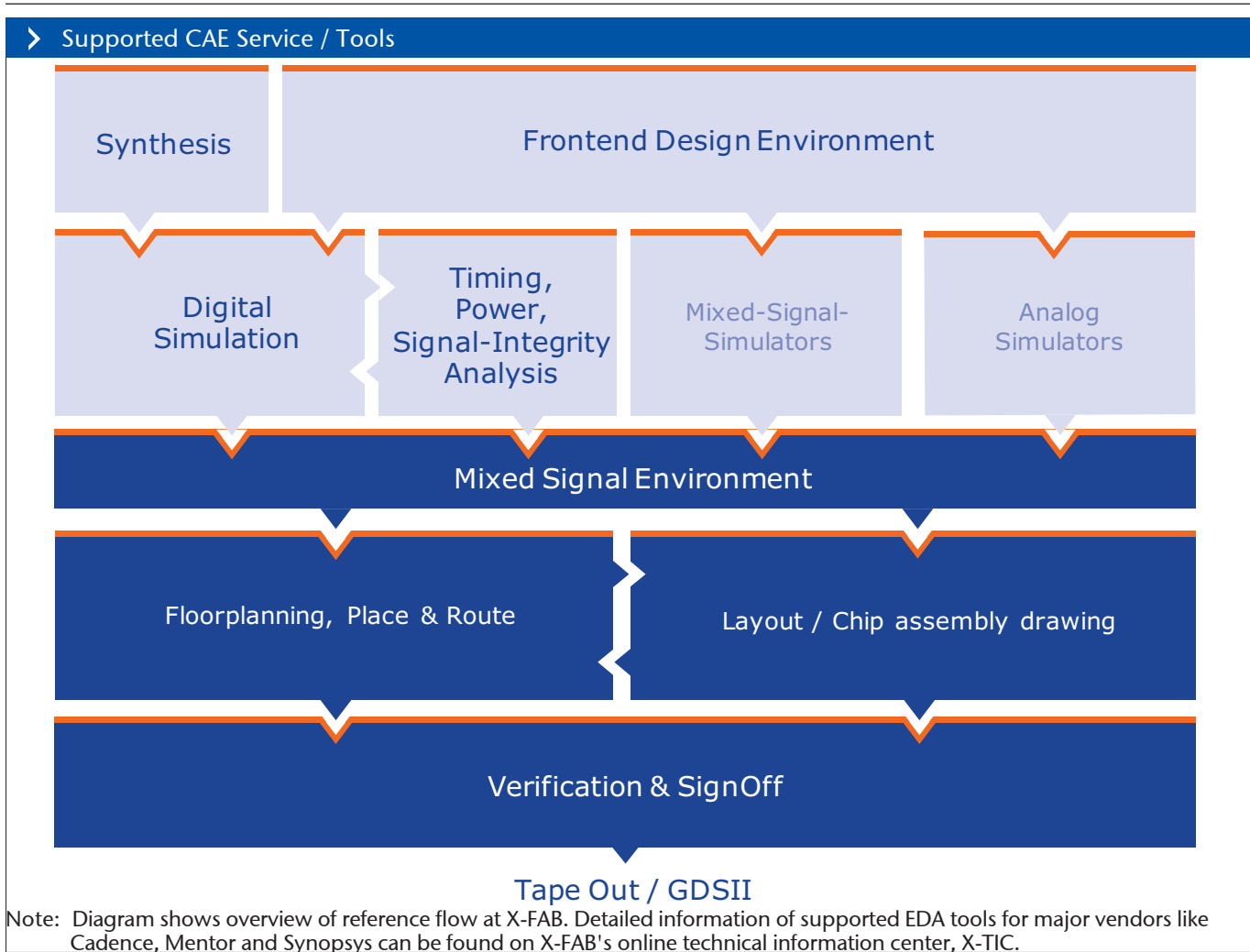


Figure 20: P+ Poly (non-salicide) Resistance Matching

> Mixed Signal Library Cells

Many logic and mixed-signal design projects are started in old technologies because designers want to re-use existing analog cells. For easy migration

to X-FAB's high performance FC025 process an increasing number of general purpose analog cells will be provided.



0.25µm Process	Mentor	Synopsys	Cadence
Foundry process (F)	Calibre DRC/LVS Calibre xRC	Hercules DRC/LVS Star-RCXT	Techfile
Foundry Compatible process (FC)	Calibre DRC/LVS Calibre xRC	Hercules DRC/LVS Star-RCXT	Techfile / Diva DRC/LVS Dracula DRC/LVS/LPE
eFlash process (eFlash)	Calibre DRC/LVS Calibre xRC	Hercules DRC/LVS Star-RCXT	Techfile / Diva DRC/LVS Dracula DRC/LVS/LPE

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> Quality Data	<p>Quality Data are available on request. Contact:</p>	<p>X-FAB Semiconductor Foundries AG Quality Assurance Haarbergstr. 67 99097 Erfurt, Germany</p>
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