### Description

The FC025 series is X-FAB’s 0.25-micron Modular Logic and Mixed Signal Technology. Main target applications are standard cell, semi-custom and full custom designs for consumer and communication products. Based upon an industry standard single poly with up to five metal layers 0.25-micron drawn gate length N-well process, modules are available for five layers of metal, double poly/metal capacitors, high resistive poly and dual gate oxide (5V) transistors.

### Key Features

- 2.5V Logic Layout & performance compatible with the industry standard
- 0.25-micron single poly, up to five metal N-well CMOS basic process
- Five layer metal options for high density circuits
- Double Poly/Metal Capacitor
- Salicided source & drain
- Direct STI
- Deep N-well module
- 2.5V Core, 3.3V/5V tolerant I/O
- 5V Module optional
- Gate oxide thickness: 5.0V -130Å, 3.3V - 70Å, 2.5V - 50Å
- Typical and worst-case models - BSIM3v3.1 (MOS, BJT, RES, CAP)
- MOS 1/f noise characterized & included in model
- Diva, Dracula, Hercules & Calibre DRC & LVS verification decks
- Calibre-xRC & Star-RXCT LPE verification decks

### Applications

- Standard Logic/controller circuits
- Mixed signal embedded systems/ systems on a chip (SOC)
- Low power mixed signal circuits
- Embedded Flash
- CMOS Sensor controller
- Communications, consumer and industrial markets

### Quality Assurance

X-FAB spends a lot of possible effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by strict quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, ISO TS 16949*, BS7799 and other standards.

* Received letter of conformance

### Deliverables

- PCM tested wafers
- Optional production services: wafer sort, assembly and final test
- Optional Engineering services: Multi Project Wafer (MPW), Prototyping tape-outs
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development

### Digital Libraries

- Foundry-specific optimized libraries
- Standard core library for high speed digital blocks
- SP/DP SRAM, 2P RF, Diffusion ROM compilers

### Analog Libraries

- Bandgaps
- Digital-To-Analog Converters
- RC Oscillators
- Power-On-Reset
- Video DAC

### Primitive Devices

- NMOS/PMOS Transistors (2.5V, 3.3V, 5.0V)
- Bipolar Transistors
- Diodes
- Capacitors
- Resistors
Process Options

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Number of Masks</th>
<th>Remarks</th>
<th>Typical Primitive Devices Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Core (1P3M)</td>
<td>17</td>
<td>P-prime wafer, single poly, triple metal</td>
<td>2.5V/3.3V NMOS/PMOS, digital applications</td>
</tr>
</tbody>
</table>

To get the available technology options; this main module can be combined with one or more of the following additional modules:

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Number of additional Masks</th>
<th>Remarks</th>
<th>Typical Primitive Devices Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIP</td>
<td>2</td>
<td>Double polysilicon process</td>
<td>Capacitor</td>
</tr>
<tr>
<td>MIM</td>
<td>1</td>
<td>Metal-insulator-Metal process</td>
<td>Capacitor</td>
</tr>
<tr>
<td>HRPOLY</td>
<td>1</td>
<td>LPP mask</td>
<td>High value resistor</td>
</tr>
<tr>
<td>S Volt</td>
<td>2</td>
<td>RACT &amp; NW2 masks</td>
<td>5 Volt NMOS &amp; 5 Volt PMOS transistors</td>
</tr>
<tr>
<td>Deep Nwell</td>
<td>2</td>
<td>Deep Nwell implantation</td>
<td>Noise isolation</td>
</tr>
<tr>
<td>SRAM</td>
<td>1</td>
<td>7.56μm² SRAM process</td>
<td>SRAM bit cell</td>
</tr>
<tr>
<td>Metal 4</td>
<td>2</td>
<td>Additional Metal layer</td>
<td>More complex wiring</td>
</tr>
<tr>
<td>Metal 5</td>
<td>2</td>
<td>Additional Metal layer</td>
<td>More complex wiring</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Number of Masks</th>
<th>Remarks</th>
<th>Typical Primitive Devices Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>eFlash (2P3M)</td>
<td>32</td>
<td>P-prime wafer, double poly, logic with mixed signal, embedded Flash</td>
<td>2.5V/3.3V NMOS/PMOS, Smart card / MCU</td>
</tr>
</tbody>
</table>

Schematic Cross Sections

Figure 1: Process Section

Figure 2: MIM Module
Main Process Flow

CMOS Module
- Alignment
- ALIGN KEY
- deep N-well
- DNWELL
- Active area
- P-well
- N-well
- Gate Poly
- Poly
- 2.5V NMOS transistor implant
- 3.3V NMOS transistor implant
- or
- 5V NMOS transistor implant
- 5V
- 2.5V PMOS transistor implant
- N+ implant
- P+ implant
- Salicide Deposition
- Contact
- Metal 1
- Via 1
- Metal 2
- Via 2
- PIP / MIM Deposition
- CAPACITOR
- Metal 3
- Via 3
- Metal 4
- Via L
- Thick Metal 5
- THKMET
- Pads
- Back side grinding (on customer request)

Additional Modules

Mask steps
<table>
<thead>
<tr>
<th>Device</th>
<th>Available with module</th>
<th>[VT] [V]</th>
<th>IDS [μA/μm]</th>
<th>[BVDSS] [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS 2.5V</td>
<td>core</td>
<td>0.53</td>
<td>600</td>
<td>&gt; 5</td>
</tr>
<tr>
<td>PMOS 2.5V</td>
<td>core</td>
<td>-0.53</td>
<td>-270</td>
<td>&lt; -5</td>
</tr>
<tr>
<td>NMOS 3.3V</td>
<td>3.3V I/O</td>
<td>0.53</td>
<td>580</td>
<td>&gt; 6</td>
</tr>
<tr>
<td>PMOS 3.3V</td>
<td>3.3V I/O</td>
<td>-0.83</td>
<td>-230</td>
<td>&lt; -6</td>
</tr>
<tr>
<td>NMOS 5V</td>
<td>SV I/O</td>
<td>0.83</td>
<td>530</td>
<td>&gt; 7</td>
</tr>
<tr>
<td>PMOS 5V</td>
<td>SV I/O</td>
<td>0.82</td>
<td>-240</td>
<td>&lt; -7</td>
</tr>
</tbody>
</table>

**Passive Devices** (typical data)

<table>
<thead>
<tr>
<th>Device</th>
<th>Area Cap [fF/μm²]</th>
<th>BV [V]</th>
<th>Voltage coefficient [ppm/V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly1-Poly2</td>
<td>0.9</td>
<td>&gt;10</td>
<td>200</td>
</tr>
<tr>
<td>Metal-insulator-Metal</td>
<td>1.0</td>
<td>&gt;10</td>
<td>100</td>
</tr>
</tbody>
</table>
### Device Parameters (continued)

#### Passive Devices (typical data) (continued)

<table>
<thead>
<tr>
<th>Device</th>
<th>RS [Ω/µm]</th>
<th>Thickness [µm]</th>
<th>Max J/W [mA/µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>N+ Poly resistor (salicide)</td>
<td>5</td>
<td>0.20</td>
<td>-</td>
</tr>
<tr>
<td>P+ Poly resistor (salicide)</td>
<td>5</td>
<td>0.20</td>
<td>-</td>
</tr>
<tr>
<td>N+ Poly resistor (non-salicide)</td>
<td>190</td>
<td>0.16</td>
<td>-</td>
</tr>
<tr>
<td>P+ Poly resistor (non-salicide)</td>
<td>160</td>
<td>0.16</td>
<td>-</td>
</tr>
<tr>
<td>P+ Poly resistor high Rs (non-salicide)</td>
<td>900</td>
<td>0.16</td>
<td>-</td>
</tr>
<tr>
<td>P+ Poly resistor medium Rs (non-salicide)</td>
<td>500</td>
<td>0.16</td>
<td>-</td>
</tr>
<tr>
<td>P+ diffusion silicided resistor</td>
<td>4.0</td>
<td>0.22</td>
<td>-</td>
</tr>
<tr>
<td>P+ diffusion resistor</td>
<td>140</td>
<td>0.17</td>
<td>-</td>
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<tr>
<td>N+ diffusion silicided resistor</td>
<td>4.5</td>
<td>0.20</td>
<td>-</td>
</tr>
<tr>
<td>N+ diffusion resistor</td>
<td>65</td>
<td>0.15</td>
<td>-</td>
</tr>
<tr>
<td>N-well resistor</td>
<td>1100</td>
<td>1.5</td>
<td>-</td>
</tr>
<tr>
<td>Deep N-well resistor</td>
<td>500</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Metal 1</td>
<td>0.08</td>
<td>0.44</td>
<td>1</td>
</tr>
<tr>
<td>Metal 2</td>
<td>0.06</td>
<td>0.44</td>
<td>1</td>
</tr>
<tr>
<td>Metal 3</td>
<td>0.06</td>
<td>0.44</td>
<td>1</td>
</tr>
<tr>
<td>Metal 4</td>
<td>0.06</td>
<td>0.44</td>
<td>1</td>
</tr>
<tr>
<td>Metal 5 (top metal)</td>
<td>0.04</td>
<td>0.85</td>
<td>1.6</td>
</tr>
</tbody>
</table>

---

### Digital Core Library Cells

ARM Standard cells up to 70K gates/mm²
6T SRAM Cell: 7.56µm² & 10.95µm²

Memory Compilers:
- ARM – SP & DP SRAM Compiler
- ARM – 2P RF Compilers
- ARM – Diffusion ROM Compiler

<table>
<thead>
<tr>
<th>eFlash Macro</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP Macro</td>
<td></td>
</tr>
<tr>
<td>AF16K8AF25</td>
<td>16K x 8</td>
</tr>
<tr>
<td>AF32K8AF25</td>
<td>32K x 8</td>
</tr>
<tr>
<td>AF32K8BF25</td>
<td>32K x 8</td>
</tr>
<tr>
<td>AF64K8AF25</td>
<td>64K x 8</td>
</tr>
<tr>
<td>AF64K8BF25</td>
<td>64K x 8</td>
</tr>
<tr>
<td>AF128K8GF25</td>
<td>128K x 8</td>
</tr>
<tr>
<td>AF256K8CF25</td>
<td>256K x 8</td>
</tr>
<tr>
<td>AF256K16FF25</td>
<td>256K x 16</td>
</tr>
</tbody>
</table>

---

### Digital I/O Cells

The digital I/O library contains a comprehensive range of I/O cells divided into distinct inputs, outputs and bidirectional variants for single voltage and dual voltage devices.

The digital I/O library has the following features:
- ARM – Integral I/O (90nm pitch)
- ARM – GPIO (60um pitch)
- ARM – USB 1.1 IO
- ARM – 5V tolerant I/O cells are available.
See section “Device Parameters” for details.

X-FAB’s CAE support kit Cadence PDK.

X-FAB supports BSIM3 models as the present SPICE model standard for MOS transistors. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence. These resistances have to be simulated with the 3-terminal SPICE JFET model.

Model sets for most popular analog simulators, e.g. Spectre, HSPICE and PSPICE are provided.

Examples for measured and modeled parameter characteristics

CMOS and Bipolar Transistor Output Characteristics

Figure 3: 2.5V NMOS Output Characteristic

Figure 4: 3.3V NMOS Output Characteristic

Figure 5: 3.3V NMOS Output Characteristic

Figure 6: 3.3V PMOS Output Characteristic

Figure 7: 2.5V Native NMOS

Figure 8: 3.3V Native NMOS
Examples for measured and modeled parameter characteristics (continued)

Figure 9: 2.5V BJT (Emitter size 2x2 μm²) Gummel Plot
Figure 10: Gain vs collector current

Figure 11: 3.3V BJT (Emitter size 2x2 μm²) Gummel Plot
Figure 12: Gain vs collector current

Matching

Figure 13: 2.5V NMOS Vt Matching
Figure 14: 2.5V PMOS Vt Matching

Figure 15: 3.3V NMOS Vt Matching
Figure 16: 3.3V PMOS Vt Matching
Examples for measured and modeled parameter characteristics (continued)

Resistor Matching

Figure 17: N+ Poly Resistance Matching

Figure 18: P+ Poly Resistance Matching

Figure 19: N+ Poly (non-salicide) Resistance Matching

Figure 20: P+ Poly (non-salicide) Resistance Matching

Mixed Signal Library Cells

Many logic and mixed-signal design projects are started in old technologies because designers want to re-use existing analog cells. For easy migration to X-FAB’s high performance FC025 process an increasing number of general purpose analog cells will be provided.
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Supported CAE Service / Tools

- **Synthesis**
- **Digital Simulation**
- **Frontend Design Environment**
  - Timing, Power, Signal-Integrity Analysis
  - Mixed-Signal Simulators
  - Analog Simulators
- **Mixed Signal Environment**
- **Floorplanning, Place & Route**
- **Layout / Chip assembly drawing**
- **Verification & SignOff**

**Tape Out / GDSII**

Note: Diagram shows overview of reference flow at X-FAB. Detailed information of supported EDA tools for major vendors like Cadence, Mentor and Synopsys can be found on X-FAB's online technical information center, X-TIC.

<table>
<thead>
<tr>
<th>0.25μm Process</th>
<th>Mentor</th>
<th>Synopsis</th>
<th>Cadence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Foundry process (F)</td>
<td>Calibre DRC/LVS Calibre xRC</td>
<td>Hercules DRC/LVS Star-RCXT</td>
<td>Techfile</td>
</tr>
<tr>
<td>Foundry Compatible process (FC)</td>
<td>Calibre DRC/LVS Calibre xRC</td>
<td>Hercules DRC/LVS Star-RCXT</td>
<td>Techfile / Diva DRC/LVS Dracula DRC/LVS/LPE</td>
</tr>
<tr>
<td>eFlash process (eFlash)</td>
<td>Calibre DRC/LVS Calibre xRC</td>
<td>Hercules DRC/LVS Star-RCXT</td>
<td>Techfile / Diva DRC/LVS Dracula DRC/LVS/LPE</td>
</tr>
</tbody>
</table>

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