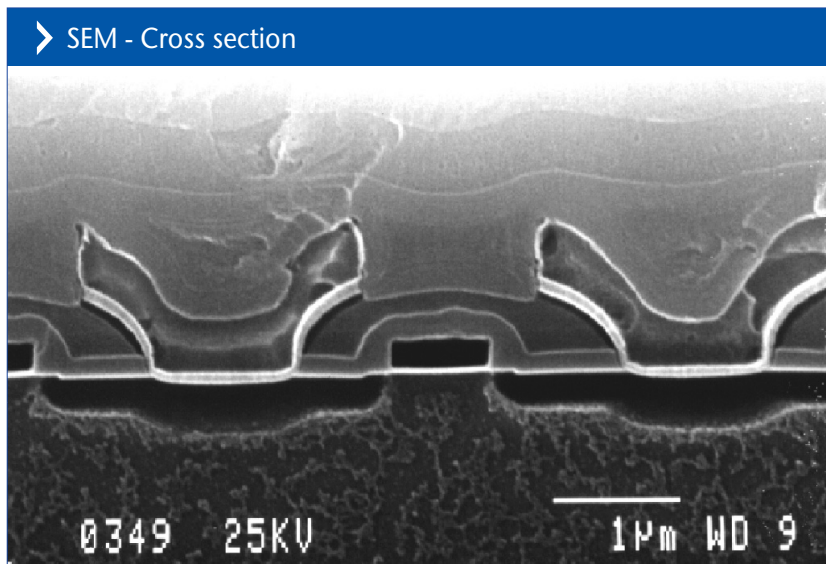
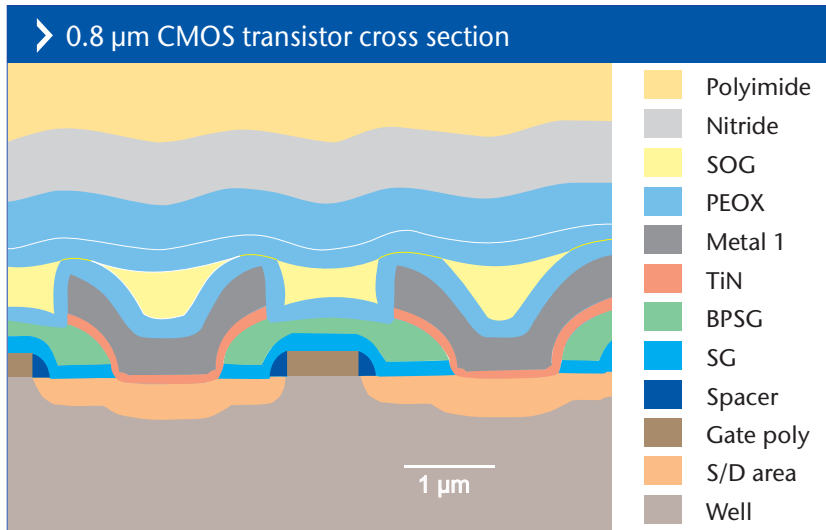


# 0.8 $\mu\text{m}$ CMOS Process Family

## > CX08

### State-of-the-art 5V 0.8 $\mu\text{m}$ CMOS Technology with additional options:

- > Analog elements: linear capacitor, high ohmic resistor
- > High voltage module: different n- and p-type, MOSFETs up to 50V, bipolar transistors available



### > Main Process Flow

P substrate

N substrate on demand

Twin well

$$X_{jn} = 3.5 \mu\text{m}$$

$$X_{jp} = 2.5 \mu\text{m}$$

Active area formation

Gate formation

$$T_{\text{GOX}} = 170 \text{ \AA}$$

N-channel LDD spacer

$$L_{\text{effn}} = 0.6 \mu\text{m}$$

$$L_{\text{effp}} = 0.8 \mu\text{m}$$

Interlayer dielectric

SG/BPSG

Metal layer 1

TiN barrier /  
RTP contact salicide  
5000  $\text{\AA}$  AlSiCu

Intermetal dielectric

SOG etchback

Metal layer 2

Ti + 10000  $\text{\AA}$  AlSiCu

Oxide/Nitride passivation

# 0.8 μm CMOS Process Family

## > CX08<sub>xy</sub>

- Combination of different modules xy gives 11 different process flows, well established in the 6-inch production line in Erfurt
- Full compatible 5V CMOS core module in all combinations
- Competitive performance, stable process in volume production
- SPICE models: BSIM3 available
- Standard cell library available
- RAM, ROM, DPRAM compiler available

Typical 5V CMOS Parameters			
Parameter WxL = 50x0.8 μm <sup>2</sup>	Unit	n-channel	p-channel
VT	V	0.75	- 0.80
IDS	mA/μm	0.4	0.20
BVDSS	V	12	- 12
ISUB	μA/μm	0.8	

Analog Elements	
Poly poly capacitor:	
Capacitance	0.86 fF/μm <sup>2</sup>
Equivalent oxide thickness	40 nm
Linearity	< 100 ppm
High ohmic resistor:	
Sheet resistance	1.2 kΩ/□
Temperature coefficient	-1.2•10 <sup>3</sup> /K

High Voltage Elements			
	Unit	n-channel	p-channel
Breakdown voltage	V	65	55
Saturation current	μA/μm	170	85
On resistance	kΩ•μm	30	70

Design Rules	
Parameter	Pitch [μm]
Gate	1.7
Metal 1	2.1
Metal 2	2.3
Active Area	2.2
Well	10.0
Contact	1.7
Via	2.0
Enclosure:	
Cont - M1	0.5
M1 - Via	0.5



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