

> CX08

0.8 Micron Modular Mixed Signal Technology

> Description

The CX08 Series is X-FAB's 0.8 Micron Modular Mixed Signal Technology. Main target applications are standard cell, semi-custom and full custom designs for Industrial, Telecommunication and Automotive products - including the 42V board net.

Based on a state of the art single poly double metal 0.8-micron drawn gate length N-well process for digital application, various process modules are available for high performance analogue and high voltage circuits.

Reliable design rules, precise SPICE models, analogue and digital libraries, IP's and development kits support the process for major CAE vendors.

> Key Features

- 0.8-micron single poly, double metal N-well core process with 11 masks
- Double poly module for poly-poly capacitors (one additional mask)
- High-resistive poly resistor module (one additional mask)
- High-voltage option up to 50V DC for HV NMOS, PMOS, DMOS, JFET and bipolar devices (four additional masks) with advanced EMC and latch-up immunity and reduced substrate noise due to triple well concept
- Extended high-voltage module - NMOS, PMOS, DMOS for 42V board net automotive application
- EEPROM module for NV-latches
- Power-metal option (third metal) for smart power applications (two additional masks)
- Large number of primitive elements
- High precision BSIM3V3 SPICE models
- Excellent analogue performance with accurate device matching
- Various digital core cell libraries optimised for most typical applications
- 1200 to 1500 effective gates per mm^2
- Typical gate delays (digital) of 160 ps
- 5V and 3.3V I/O cell libraries
- IEEE 1149.1 boundary scan macros
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Analogue library
- High-density RAM, DPRAM. ROM blocks
- OTP options: poly-fuses, zener-zaps
- Development kits for major EDA tools
- Megafunctions and IP's available

> Applications

- Mixed signal embedded systems; systems on a chip (SOC)
- High precision mixed signal circuits
- Low-power mixed signal circuits
- Analogue frontends for sensors
- Circuits with integrated high voltage I/O's and voltage regulators
- Instrumentation
- AD/DA Converters
- Communications, automotive and industrial markets

> Quality Assurance

X-FAB spends every possible effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of them guided by

rigorous quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS 16 949 and other standards.

> Deliverables

- PCM tested wafers
- Optional production services: wafer sort, assembly and final test
- Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Service (MLM)
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development
- Second source available

> Digital Libraries

- Foundry-specific optimized libraries
- Standard core library for high speed digital blocks
- Low-power library, 50% less power, 40% less area
- Isolated library for reduced substrate noise and improved EMC
- IEEE 1365 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models
- Synthesis libraries
- IDDQ libraries
- Macrofunction and IP's on request
- RAM, DPRAM, ROM
- Poly fuses, Zener zaps
- NV latches

> Analog Libraries

Primitive Devices	Analog Magefunctions
NMOS/PMOS Transistors	Digital to Analog Converters
HV NMOS/PMOS Transistors	Analog to Digital Converters
DMOS Transistors	
JFETs	
NPN/PNP Bipolar Transistors	
Diodes	
Capacitors	
Polysilicon and Diffusion Resistors	

Module Name	No. of Masks	Remarks	Typical Primitive Devices Applicaitons
CMOS core	11	Single poly, double metal CMOS	5V NMOS/PMOS bipolars, resistors

The core module can be combined with one or more of the following additional modules:

Module Name	No. of Masks	Remarks	Typical Primitive Devices Applicaitons
high voltage CMOS	4	triple well (isolated p-well) dual gate oxide	HV NMOS/PMOS additional bipolars, diodes
extended high voltage CMOS	1	optimized technology for improved mid-oxide high voltage transistors	80V HV NMOS/PMOS 42V automotive board net
EEPROM	2	double poly, patented non-volatile-memory cell	NV Latches double poly capacitor
poly1-poly2 capacitor	1	double poly, alternatively for EEPROM module	double poly capacitor analog
high resistive poly	1	selectively doped single poly	high ohmic resistor analog
ESD implant	3	ESD implant	5V ESD-NMOS 5V-I/Os with ESD robustness up to 8kV
triple metal	2	additional metal layer	more complex wiring
power metal	2	thick third metal, alternatively for triple metal module	reduced internal resistance, higher currents
optical window	1	oxide window	optical applications

> Main Process Flow



> Schematic Cross Sections

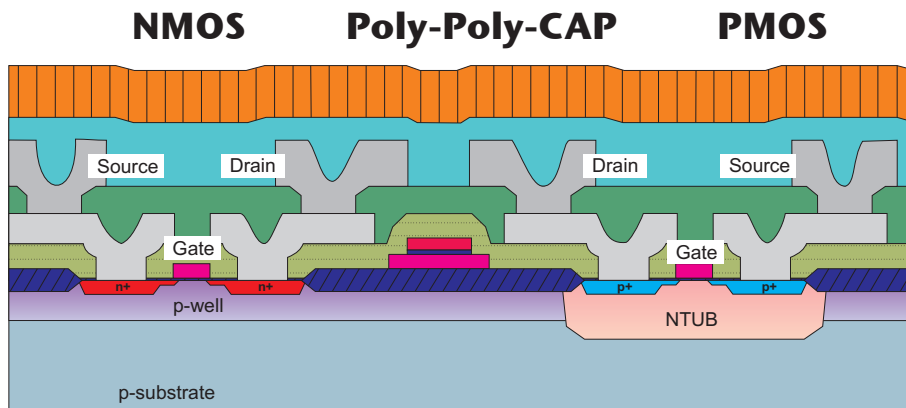


Figure 1: 5V devices

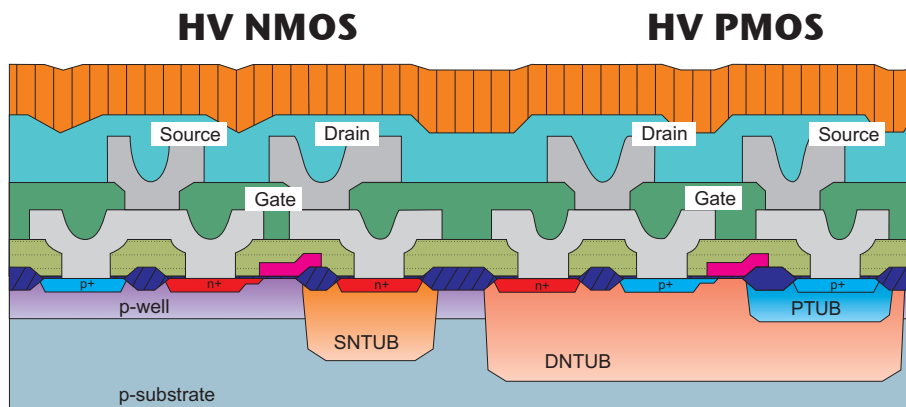


Figure 2: High Voltage devices with power metal

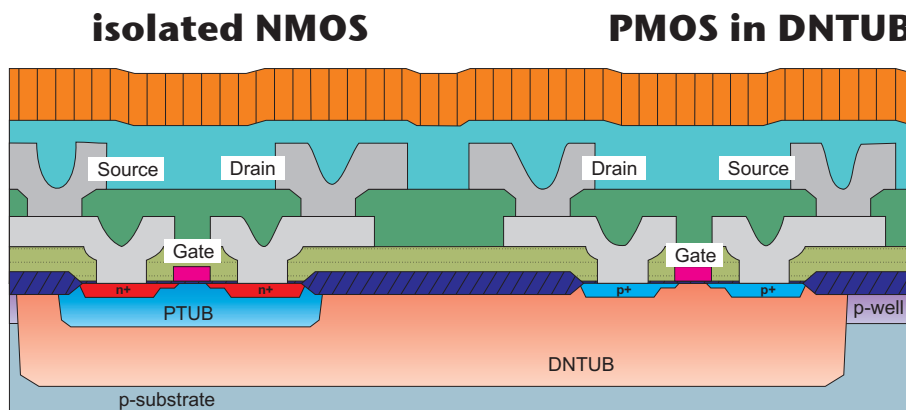


Figure 3: Isolated 5V devices

> Basic Design Rules

Mask	Width [μm]	Spacing [μm]
Standard N-well	5.0	5.0
HV deep N-well	5.0	11.0
HV shallow N-well	5.0	7.0
Isolated P-well	3.0	5.4
Active Area	0.8	1.4
Poly-Silicon Gate	0.8	0.9
Contact	0.8	0.8
Metal 1	1.1	1.0
Via 1	0.9	1.0
Metal 2 / Metal 3	1.2	1.1
Via 2	1.6	1.6
Metal 3 (Power Metal)	3.0	3.0

> Device Parameters

The following devices can be used for circuit designs. They are well characterised and part of a primitive device library. The device names correspond with the SPICE model names. They all have been qualified.

Different reliability tests gave the maximum allowed operating conditions; the values in brackets denote absolute maximum ratings. See also the availability with different options.

Active Devices (typical data)

MOS Transistor							
Device	Device Name	Available with module	VT [V]	IDS [$\mu\text{A}/\mu\text{m}$]	BVDS [V]	max. VDS [V]	max. VGS [V]
NMOS 5V	NMOS4	CORE	0.72	380	13	5.5	5.5
PMOS 5V	PMOS4	CORE	0.80	185	12	5.5	5.5
Isolated NMOS	NMOSPW	HV	0.68	380	13	5.5	5.5
PMOS in HV well	PMOSNWD	HV	0.80	185	12	5.5	5.5
High voltage NMOS	NMOSMH	HV	1.80	170	65	40	20
High voltage PMOS	PMOSMH	HV	1.90	75	55	36	20
High Voltage NDMOS	NMOSMD	HV	2.00	190	80	50	20
Extended HV NMOS	NMHE	XHV	1.95	140	95	60	20
Extended HV PMOS	PMHE	XHV	0.85	140	80	60	20
Extended HV DMOS	NMDSE	XHV	1.95	200	80	60	20

Note: The listed devices are examples only.

Bipolar Transistors							
Device	Device Name	available only with	VBE [mV]	BETA	VA [V]	BVCEO [V]	Max VCE [V]
Vertical PNP, Collector on Bulk	VERT15		660	12	> 100	> 7	5.5
Isolated Lateral PNP	LAT3		620	90	12	> 7	5.5
Vertical PNP, Collector on Bulk	VERT5H	HV	670	70	> 80	50	40
Isolated Vertical NPN	VERTN1	HV	650	200	30	40	10

Junction FETs								
Device	Device Name	available only with	Vpinch [V]	max VDB [V]	BVDSS [V]	IDS [μA]	RON [$\text{k}\Omega$]	note
Pinched N-Well Resistor	RNPINCH	HV	4	30 (35)	40	7		per μm width
N-Channel Junction FET	NJFET10	HV	4	50 (55)	60	1200	2.5	fixed layout

> Device Parameters (continued)

Passive Devices (typical data)

Capacitors							
Device	Device Name	available only with	Area Cap [fF/ μm^2]	BV [V]	Voltage coefficient [ppm/V]	Temp. coefficient [$10^{-3}/\text{K}$]	Max VCC [V]
POLY1-MET1-MET2 Sandwich	CSANDWT		0.09				50 (55)
DNTUB-POLY1-MET1-MET2 Sandwich	CSANDW	HV	0.18				50 (55)
Poly1-Poly2	CPOLY	Poly2	0.86	30	30	0.03	5.5 (7)

Resistors and Conductors							
Device	Element	available only with	RS [Ω/\square]	Thickness [μm]	Temp. coefficient [$10^{-3}/\text{K}$]	Max Current Density [mA/ μm]	Max VTB [V]
Poly Silicon	POLY1		32	0.30	0.7	0.45	50 (55)
	POLYH	High Res	1200	0.30	-1.2	0.18	50 (55)
	POLYM	High Res	130	0.30	0.35	0.40	50 (55)
	POLY2	Poly 2	33	0.30	0.7	0.45	50 (55)
Diffusion	NDIFF		42	0.30	1.5		8 (10)
	PDIFF		55	0,50	1.6		8 (10)
Well	NWELL		650	4.0	6.3		8 (10)
	DNTUB	HV	600	7.0	6.3		50 (55)
	SNTUB	HV	2300	5.5	6.5		50 (55)
	PWELL	HV	5000	1.6	4.6		45 (50)
Metal	MET1		0.07	0.7	3.0	0.9	30
	MET2		0.035	1.0	3.0	3.0	60
	MET3	met 3	0.012	2.3		7.0	60

> Digital Core Cells

X-FAB provides different core cells optimised for most typical applications. The standard core library includes more than 200 cells. Functionality and layouts are optimised for best synthesis results in high speed applications. The low power library offers 130 cells optimised for low power and area. These cells are most suitable for blocks running up to 100 MHz clock frequency.

Both standard and low power libraries are available in an "isolated" version. NMOS devices are placed in P-wells. The P-wells are placed in deep N-wells. Therefore NMOS devices do not have a common bulk.

The main advantages of isolated libraries are:

- Reduced substrate noise
- Superior latch-up and EMC immunity
- Bulk potential independent from substrate

These libraries are most suitable for low-noise mixed-signal applications and for products with high EMC requirements, such as automotive IC's.

"Isolated" libraries require HV process option. If HV option is not used, substrate noise can be reduced by using separate bulk wire library.

Name	Category	Density ¹⁾	r_factor ²⁾	Main feature
D_CELLS	standard	ML3: 1.8 ML2: 1.1	ML3: 1.54 ML2: 2.50	high speed
D_CELLS_FL	junction isolated	ML3: 1.2 ML2: 0.7	ML3: 1.54 ML2: 2.50	high speed, junction isolated ^{3,4)} , low noise, voltage shifting
D_CELLSL	low power	ML3: 3.5 ML2: 2.0	ML3: 1.67 ML2: 2.86	low power consumption
D_CELLSL_B	low power, low noise	ML3: 2.8 ML2: 1.6	ML3: 1.67 ML2: 2.86	low power consumption, low noise
D_CELLSL_FL	low power, junction isolated	ML3: 2.0 ML2: 1.2	ML3: 1.67 ML2: 2.86	low power consumption, junction isolated ^{3,4)} , low noise, voltage shifting

> Digital Core Cells (continued)

- 1) averaged value: kGE/mm^2 (GE = NAND2 Gate Equivalent)
ML2: 2 metal layer routing
ML4: 4 metal layer routing
- 2) average value: $r_factor = Routing_factor$
 $Place\&Route_area = Cell_area * Routing_factor$
- 3) NMOS, PMOS with seperated bulk supply
- 4) only available in cx08h technology (high voltage):
The junction isolated library is recommended for mixed-signal high voltage applications and noise sensible applications. The junction isolation provides two advantages: Firstly the junction isolation allows to shift the library ground supply voltage up the high voltage level minus the library power supply voltage. Secondly the switching noise of the junction isolated digital cells does not affect the silicon substrate.

ML3: 3 metal layer routing

> Digital I/O Cells

I/O cells are available for 5 V and 3.3 V operation voltage. Two I/O ring systems are available for pad-limited and for core limited designs. Pad-limited cell height is 514.6 μm with 115 μm bond pad pitch. I/O

cells for core limited design have 231.3 μm height with variable bond pad pitch (>200 μm).

The digital I/O library has the following features:

Name	Category	Main feature
IO_CELLS	standard	Pad limited (x < y)
IO_CELLS_F	standard	Core limited (x > y)
IO_CELLS_JI	junction isolated ^{3,4)}	Pad limited (x < y)

Input	CMOS	TTL	Pull-up	Pull-down	Output	
Standard Input	■	■	■	■		
Schmitt-Trigger	■	■	■	■		
Bi-directional	■	■	■	■	1 - 8 mA (24 mA)	
Slew-Rate Control Option	■	■		■	4 - 8 mA (24 mA)	
Output	1 mA	2 mA	4 mA	8 mA	16 mA	24 mA
Standard	■	■	■	■	■	■
Slew-Rate Control Option			■	■	■	■
3-State	■	■	■	■	■	■
Open Drain	■	■	■	■	■	■

> Analog Library Cells

Many analogue and mixed-signal design projects are started in old technologies because designers want to re-use existing analogue cells.

For an easy migration to X-FAB's high performance CX08 process an increasing number of general purpose analogue cells are provided.

ADC / DAC							
Name	Function	Principle	Resolution [Bits]	Accuracy [LSB]	Conversion time [μs]	Supply current [μA]	Comment
ADC10	ADC	successive approximation	10	± 0.5	11	860	Sample & Hold
ADC8	ADC	successive approximation	8	± 0.5	9	1000	Sample & Hold
DAC8	DAC	Resistor strings	8	± 0.5	1	150	
DAC10	DAC	Resistor strings	10	± 0.5	1	200	

> Analog Primitive Devices and Models

A very wide range of different analogue primitives enable analogue designers to develop sophisticated, high precision, reliable analogue and high voltage circuits. See section "Devices and their operating conditions" for details.

High performance process modules, well defined primitives devices and accurate device models are the key success factors for analogue and mixed-signal design. Combined with X-FAB's CAE support kit "TheKit" and state of the art design methodologies first right analogue mixed-signal designs are reality.

X-FAB supports BSIM3 models as the present SPICE model standard for MOS transistors. Bipolar transistors are modelled using the Gummel-Poon model for a given emitter size. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence.

These resistances have to be simulated with the 3-terminal SPICE JFET model.

Model sets for most popular analogue simulators, e.g. Spectre, HSPICE and PSPICE are provided.

The same characterisation and modelling effort is spent for parasitic devices and 3rd order parameters which are usually very important for analogue design.

The matching behaviour of MOS transistors, bipolar transistors, resistors and capacitors is very intensively investigated and characterised. Final matching parameters are extracted for all active and most of passive elements. These parameters are used at simulator model implementation for Monte Carlo simulation.

> Examples for measured and modeled parameter characteristics

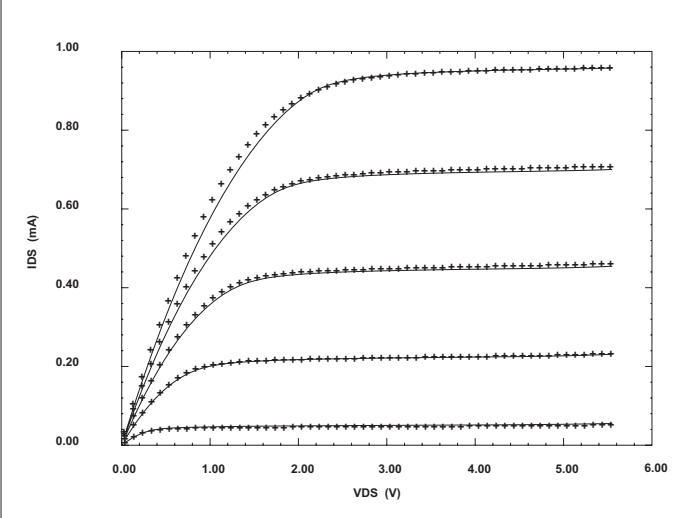


Figure 4: NMOS output characteristic
 $W/L = 3/1$, $V_{GS} = 1.4, 2.3, 3.2, 4.1, 5$ V
 + = measured, solid line = BSIM3v3 model

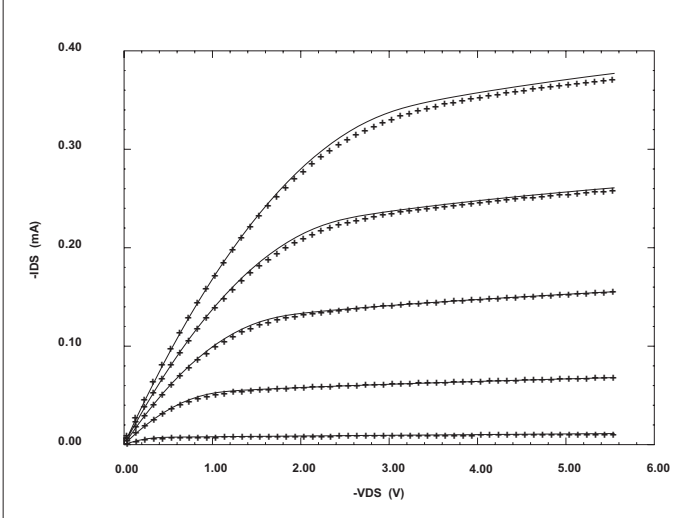


Figure 5: PMOS output characteristic
 $W/L = 3/1$, $-V_{GS} = 1.4, 2.3, 3.2, 4.1, 5$ V
 + = measured, solid line = BSIM3v3 model

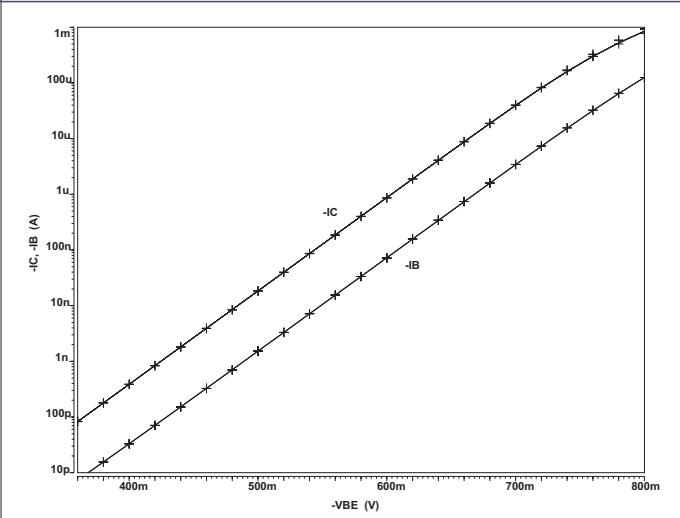


Figure 6: Gummel plot of vertical PNP bipolar transistor VERT15
 + = measured, solid line = SPICE model

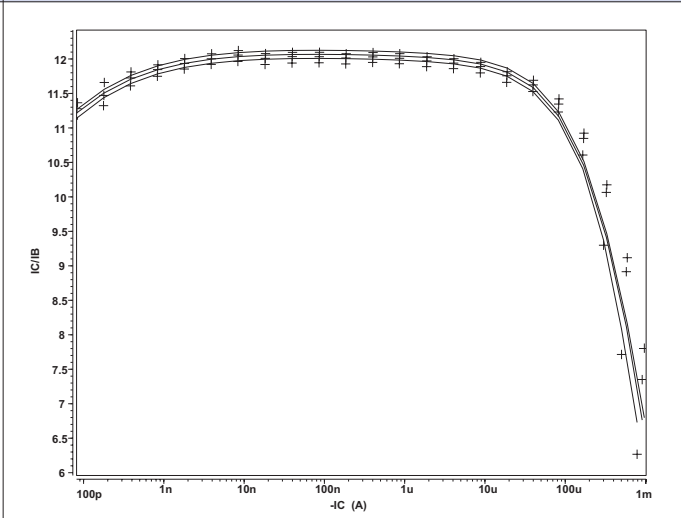


Figure 7: Current gain of vertical PNP bipolar transistor VERT15
 + = measured, solid line = SPICE model

Examples for measured and modeled parameter characteristics (continued)

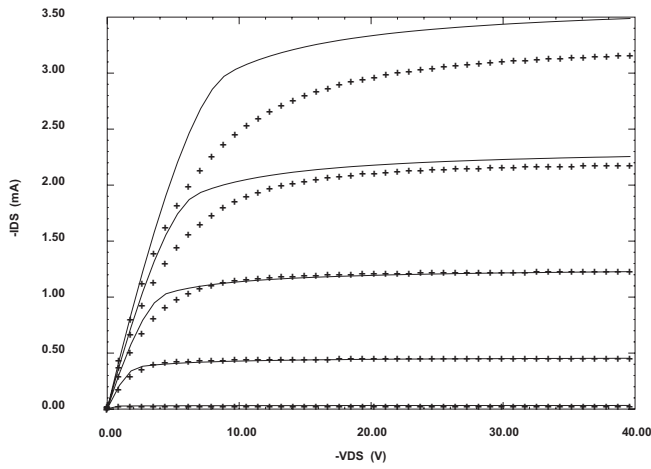


Figure 8: PMOSMH output characteristic
 $W/L = 40/3$, $-V_{GS} = 2.67, 5, 7.33, 9.67, 12$ V
 $V_{SB} = 0$ V, + = measured, solid line = BSIM3v3 model

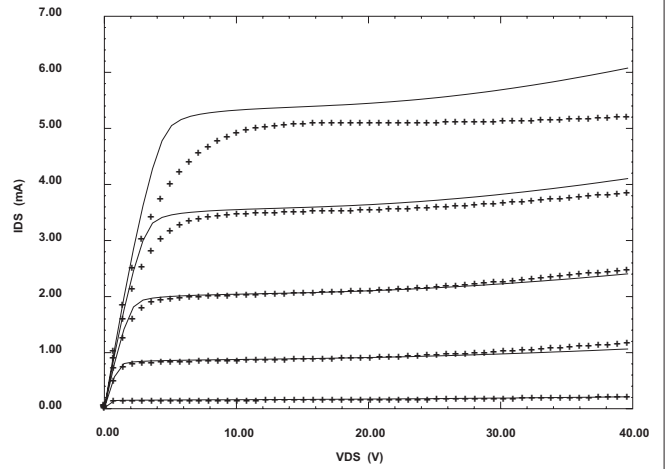


Figure 9: NMOSTD output characteristic
 $W/L = 40/2$, $V_{GS} = 1.4, 2.3, 3.2, 4.1, 5$ V
 $V_{SB} = 0$ V, + = measured, solid line = BSIM3v3 model

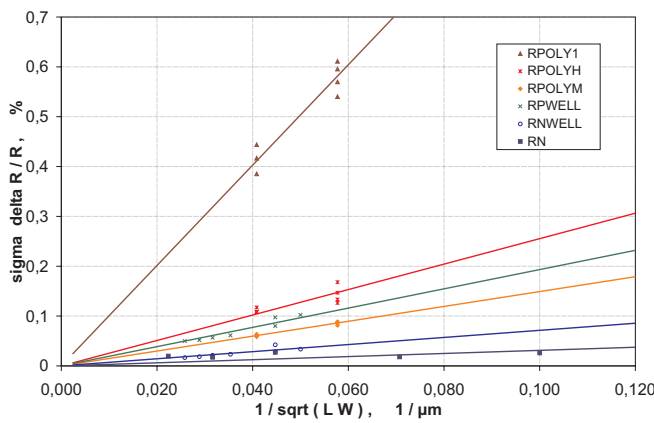


Figure 10: resistor matching

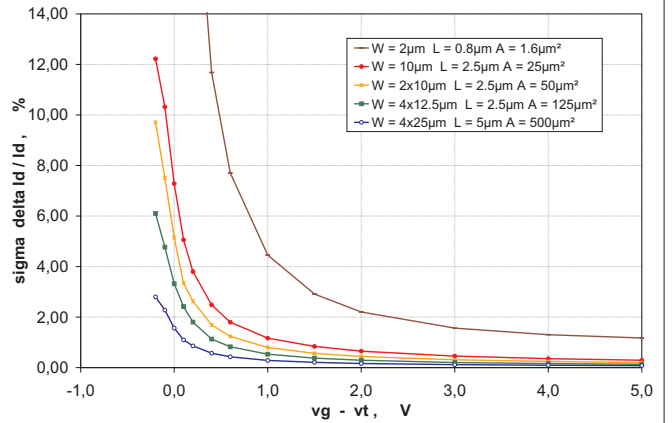


Figure 11: drain current matching NMOS4

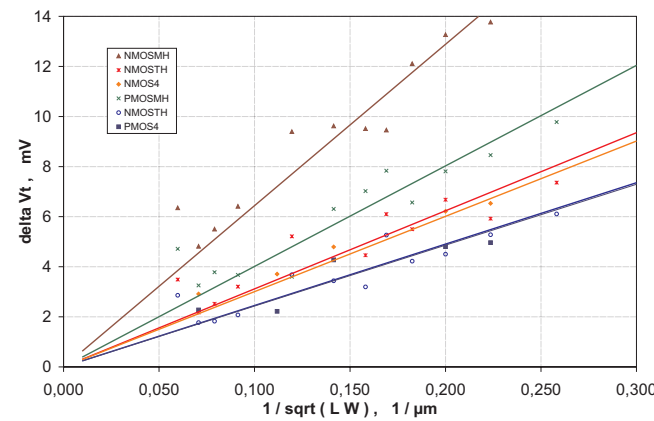
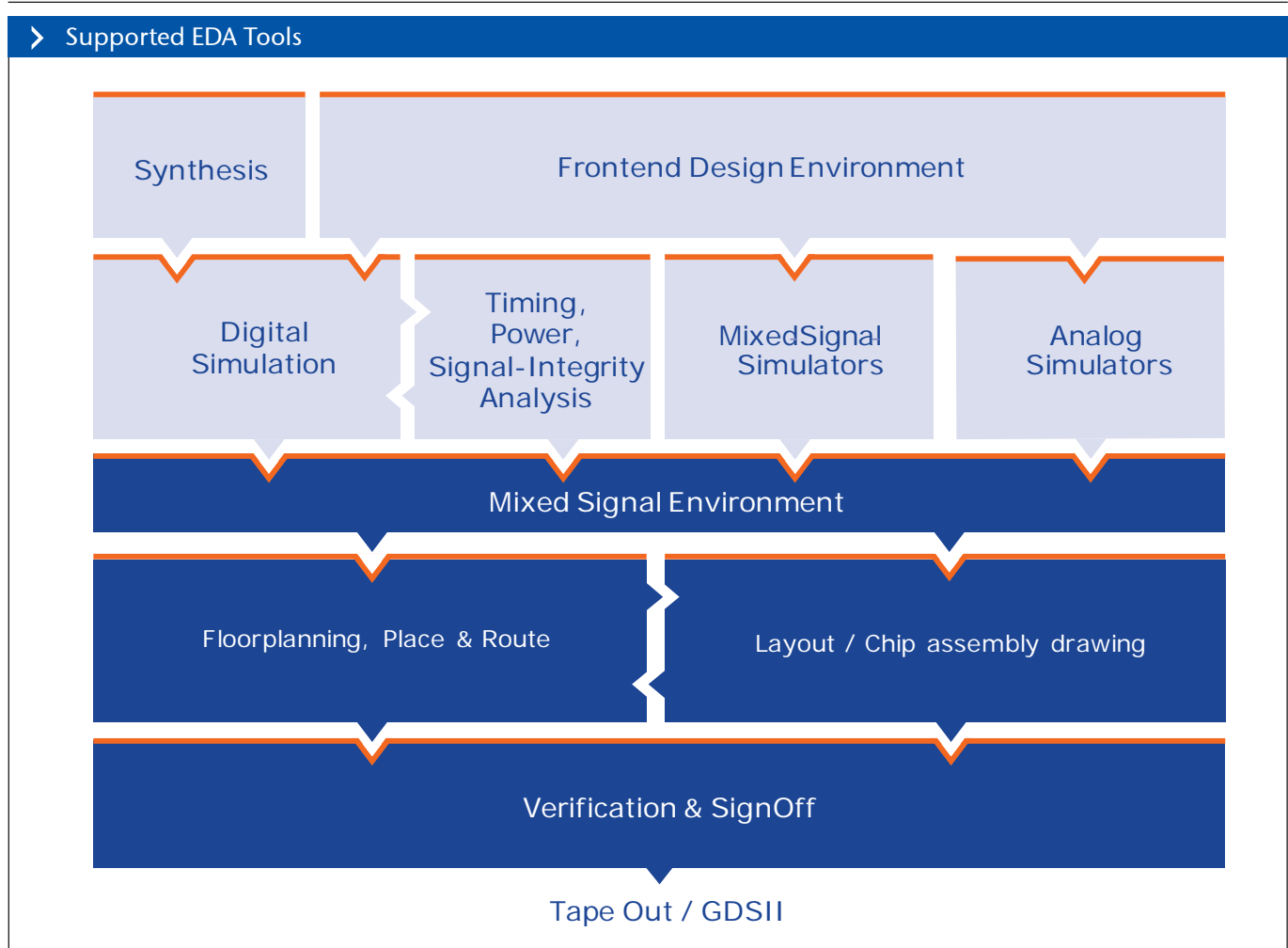


Figure 12: treshold voltage matching



> X-FAB's IC Development Kit "TheKit"

The X-FAB IC Development Kit is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well.

The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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