

0.6 μm CMOS Process Family

> CX06

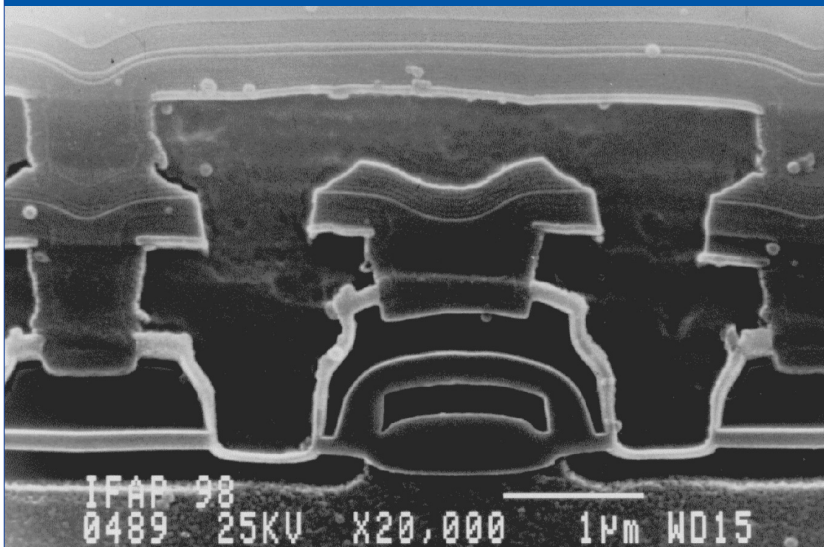
State-of-the-art 5V 0.6 μm CMOS Technology

- > Single-layer poly with double and triple layer metal option
- > Double-layer poly with double and triple layer metal option
- > Digital standard cell library
- > Analog elements
- > Memory generators (RAM, DPRAM, ROM compiler)
- > Simulation parameters (BSim3v3)

> Main Process Flow

- p substrate
- Twin well
 $X_{jn} = 2 \mu\text{m}$ / $X_{jp} = 3 \mu\text{m}$
- Active area formation
 $d_{\text{FOX}} = 580 \text{ nm}$
- Gate formation
 $d_{\text{GOX}} = 12.5 \text{ nm}$
- Poly1/Poly2-Capacitor Formation (optional)
 $C' = 0.85 \text{ fF}/\mu\text{m}^2$
- HiResPoly-Si-Resistor Formation (optional)
 $R_S = 1.2 \text{ k}\Omega/\square$
- N- and p-channel
- LDD Spacer Formation
 $L_{\text{effn}} = 0.55 \mu\text{m}$;
 $L_{\text{effp}} = 0.62 \mu\text{m}$
- Interlayer dielectric
USG/BPTEOS
- Metal layer 1
TiN barrier /
RTP contact silicide /
W plug /
500 nm hot AlCu /
TiN-ARC
- Intermetal dielectric 1
PE oxide /
SOG etchback /
PE oxide
- Metal layer 2
Ti + 500 nm hot AlCu /
TiN ARC
- Intermetal dielectric 2
PE oxide /
SOG etchback /
PE oxide
- Metal layer 3
Ti + 800 nm AlCu /
TiN ARC
- Oxinitride/Nitride passivation

> SEM - Cross section of via-contact stacks



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> CX06xy

- 5V SLP/DLM, SLP/TLM, DLP/DLM, DLP/TLM for high packing density
- 0.6 μm drawn gates for high speed and current drive
- n-channel & p-channel LDD transistors for high reliability
- Industry compatible for foundry flexibility

Process Family				
Process Name	No. of Mask Layers	Poly Capacitor Module	High Resistive Poly Module	Metal 3 Module
CX06AA	11			
CX06AD	12	■		
CX06AI	13	■	■	
CX06AQ	13			■
CX06AS	14	■		■
CX06AT	15	■	■	■

Design Rules	
Parameter	Pitch [μm]
Gate	1.4
Metal 1	1.7
Metal 2	1.7
Metal 3	2.2
Active Area	1.8
n-Well	7.8
Contact	1.2
Via 1	1.4
Via 2	1.4
Enclosure:	
Cont - M1	0.3
M1 - Via 1	0.4
M2 - Via 2	0.4
M3 - Via 3	0.4

Typical Electrical Parameters			
Parameter	Unit	n-channel	p-channel
$W \times L = 10 \times 0.6 \mu\text{m}^2$			
V_T	V	0.72	- 0.80
I_{DS}	$\mu\text{A}/\mu\text{m}$	500	250
BV_{DSS}	V	> 10	< -10

Sheet Resistances		
Layer	Unit	Value
N+	Ω/\square	32
P+	Ω/\square	60
n-Well	Ω/\square	1000
Poly-Si	Ω/\square	33
Hires Poly-Si	Ω/\square	1200



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