

0.6 μm CMOS Process

> CX06



0.6 Micron Modular Mixed Signal Technology

> Description

The CX06 Series is X-FAB's 0.6 Micron Modular Mixed Signal Technology. Main target applications are standard cell, semi-custom and full custom designs for Industrial, Automotive and Telecommunication products.

Based on a state of the art single poly double metal 0.6-micron drawn gate length N-well process for

digital application, process modules are available for triple metal and double poly high performance analogue circuits.

Reliable design rules, precise SPICE models, analogue and digital libraries, IP's and development kits support the process for major CAE vendors.

> Key Features

- 0.6-micron single poly, double metal N-well CMOS basic process
- Triple metal option for high density circuits
- Double Poly capacitor
- High-resistive Poly resistor
- High precision BSIM3V3 SPICE models for CMOS and Gummel Poon model for bipolars
- Excellent analog performance with accurate device matching
- Three different digital core cell libraries optimized for speed, low power or low noise
- Analog library
- Up to 4500 effective gates per mm^2 (3ML)
- Typical gate delays (digital) of 160ps
- 5V and 3.3V I/O cell libraries with CMOS / TTL interfacing capability
- IEEE 1149.1 boundary scan macros
- High-density RAM, DPRAM. ROM blocks
- Electrostatic discharge (ESD) protection in accordance with MIL-STD
- Optional ESD layer for higher ESD protection
- OTP options: zener-zaps
- Development kits for major EDA tools

> Applications

- Mixed signal embedded systems; systems on a chip (SOC)
- High precision mixed signal circuits
- Low-power mixed signal circuits
- Analog front ends for sensors

> Quality Assurance

X-FAB spends every possible effort to improve the product quality and reliability and to provide competent support to the customers. This is maintained by the direct and flexible customer interface, the reliable manufacturing process and complex test and evaluation conceptions, all of

them guided by rigorous quality improvement procedures developed by X-FAB. This comprehensive, proprietary quality improvement system has been certified to fulfill the requirements of the ISO 9001, QS 9000, VDA 6, ISO TS16 949 and other standards.

> Deliverables

- PCM tested wafers
- Optional production services: wafer sort, assembly and final test
- Optional Engineering services: Multi Project Wafer (MPW) and Multi Layer Mask Service (MLM)
- Optional Design services; e.g. feasibility studies, place & route, synthesis, custom block development

> Digital Libraries

- Foundry-specific optimized libraries
- Standard core library for high speed digital blocks
- Low-power library, 50% less power, 40% less area
- Low-noise library with separate bulk contacts for reduced substrate noise
- IEEE 1365 Verilog simulation models
- IEEE 1076.4 VHDL-VITAL simulation models
- Synthesis libraries
- Macrofunction and IP's on request
- RAM, DPRAM, ROM

> Analog Libraries

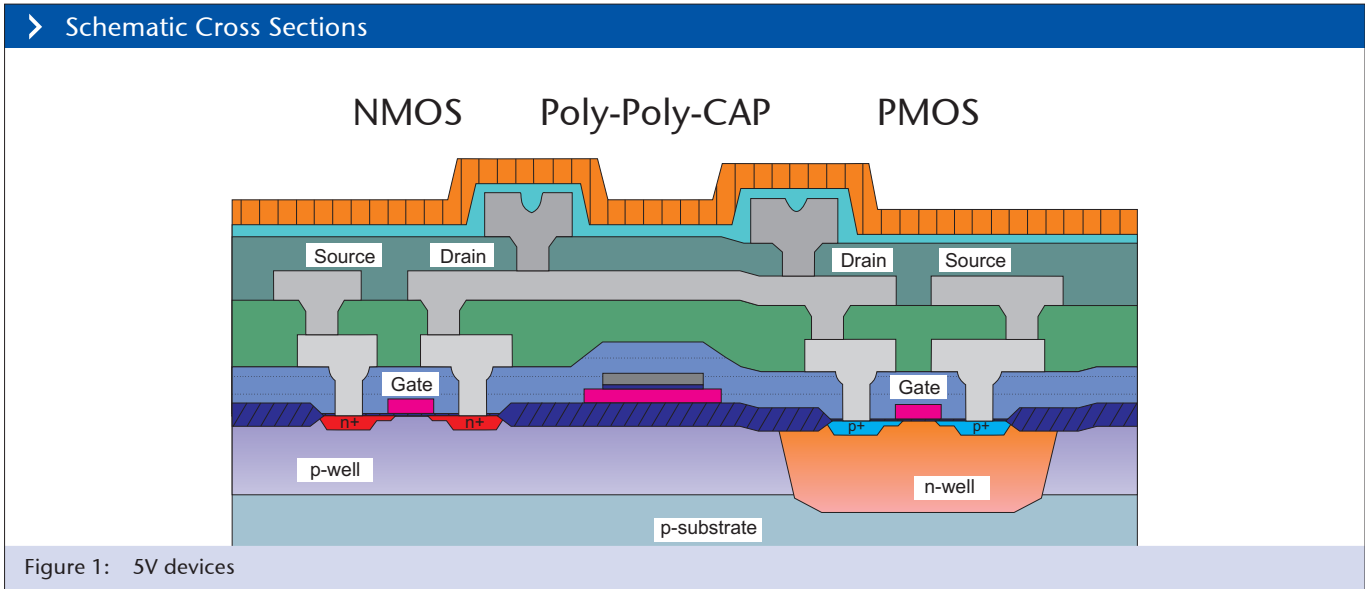
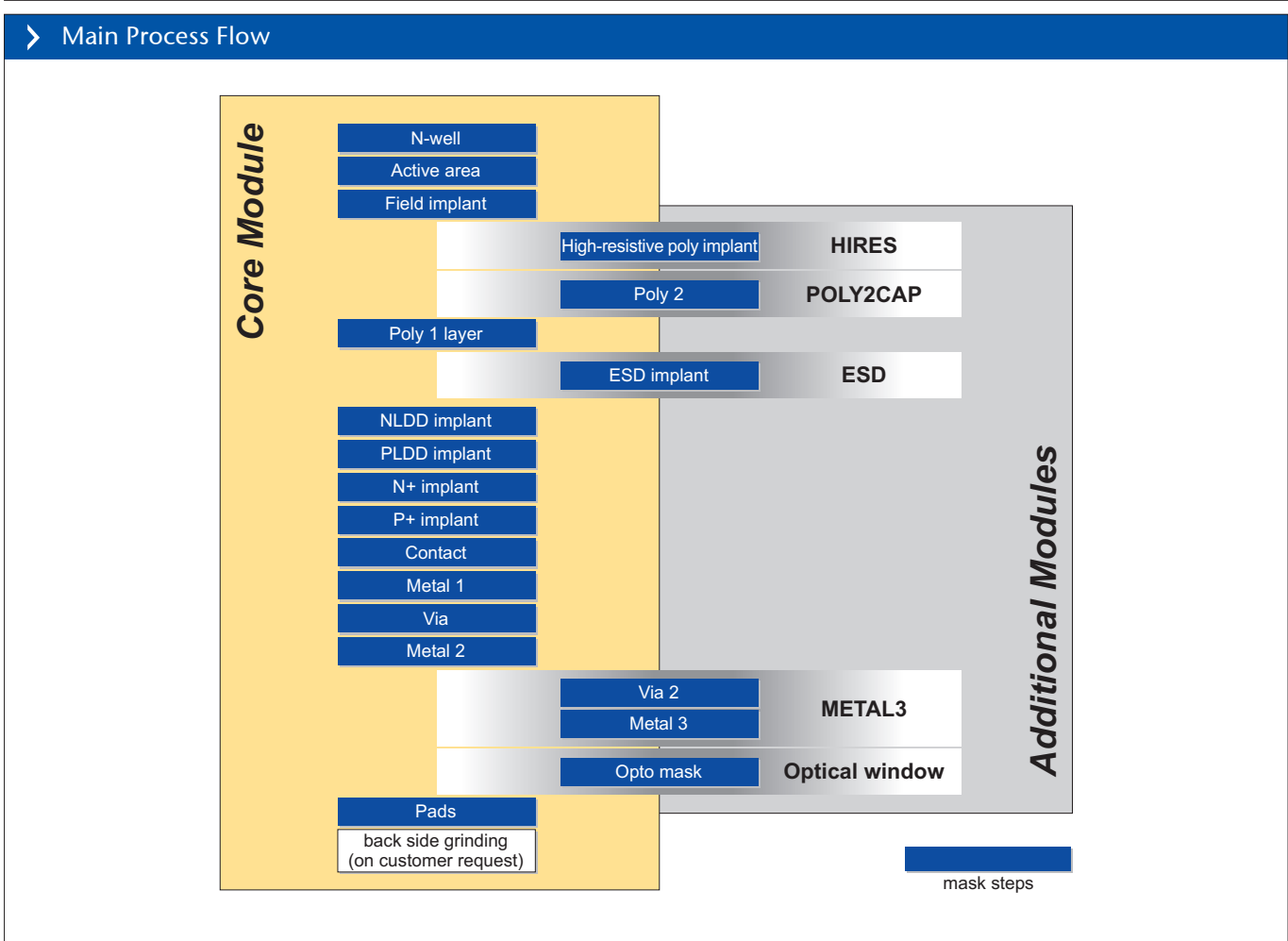
- Operational Amplifiers
- Comparators
- RC Oscillators
- Bandgaps
- Bias Cells
- Power-On-Reset
- Analogue Switches
- Crystal Oscillators
- Analog-To-Digital Converters
- Digital-To-Analog Converters
- DC / DC Converters

> Process Options

Module name	No. of masks	Remarks	Typical primitive devices applications
CMOS core module	11	5V CMOS core module, p-substrate, single poly, double metal	5V NMOS/ PMOS, bipolars, resistors

This main module can be combined with one or more of the following additional modules:

Module name	No. of add. masks	Remarks	Typical primitive devices applications
POLY2CAP	1	double poly	double poly capacitor analog
HIRES	1	single poly but selective doped	high ohmic resistor for analog applications
ESD implant	1	specific implant for ESD protection	5V ESD-NMOS, 5V-I/O's with improved ESD robustness
Optical window	1	oxide window	optical applications
METAL3	2	third metal layer	more complex wiring



Basic Design Rules		
Mask	Width [μm]	Spacing [μm]
N-well	3.0	4.8
Active Area	0.6	1.2
Poly-Silicon Gate	0.6	0.8
Poly-Silicon Resistor	0.8	0.8
Contact	0.6	0.6
Metal 1	0.9	0.8
Via 1	0.7	0.7
Metal 2	0.9	0.8
Via 2	0.7	0.7
Metal 3	1.2	1.0

> Device Parameters

The following devices can be used for circuit designs. They are well characterized and part of a primitive device library. The device names correspond with the SPICE model names.

Different reliability tests gave the maximum allowed operating conditions; Values in brackets denote absolute maximum ratings. See also the availability with different options.

Active Devices (typical data)

MOS Transistors							
Device	Device Name	Avail. only with module	VT [V]	IDS@VGS [μA/μm@V]	BVDSS [V]	Max. VDS [V]	Max. VGS [V]
NMOS 5V	NMOS	CORE	0.72	500	> 10	5.5	5.5
PMOS 5V	PMOS	CORE	-0.80	250	<-10	5.5	5.5
NMOS 10V	NMOSH	CORE	0.82	175	30	11	5.5
NMOS with ESD implant	NESD	ESD implant	0.80	500	12.5	5.5	5.5
Bipolar Transistors							
Device	Device Name	Avail. only with module	BETA	VA [V]	BVCEO [V]	Max VCE [V]	
Vertical PNP	VERT15	CORE	13	> 100	> 7	5.5	
Lateral PNP	LAT3	CORE	30	20	> 7	5.5	

Passive Devices (typical data)

Capacitors							
Device	Device Name	Avail. only with module	Area Cap [fF/μm ²]	BV [V]	Voltage coefficient [ppm/V]	Temp. coefficient [10 ⁻³ /K]	Max VCC [V]
POLY1-MET1-MET2 Sandwich	CSANDWT	CORE	0.082				40
POLY1-MET1-MET2-MET3 Sandwich	CSANDWTM	METAL3	0.11				40
Poly1-Poly2	CPOLY	POLY2CAP	0.86	30	<50	0.03	5.5
Resistors							
Device	Device Name	Avail. only with module	RS [Ω/□]	Thickness or junction depth [μm]		Temp. coefficient [10 ⁻³ /K]	Max VTB [V]
Poly1 resistor	RPOLY1	CORE	33	0.25		0.75	40
Poly2 resistor	RPOLY2	POLY2CAP	32	0.25		0.03	
High resistive poly resistor	RPOLYH	HIRES	1200	0.25		-1.05	40
P+ diffusion	RDIFFP3	CORE	60	0.2		1.65	8
N+ diffusion	RDIFFN3	CORE	32	0.3		1.8	8
NWELL resistor	RNELL	CORE	1000	2.5		6.6	8
Metal	MET1	CORE	0.1	0.67		3.0	40
	MET2	CORE	0.04	1.0 / 0.8		3.0	40
	MET3	Metal3	0.04			3.0	40

> Digital Core Library Cells

X-FAB provides three different core libraries optimized for most typical applications in mixed signal ASIC:

- The standard core library is optimized for best synthesis results in high speed applications.
- The low power library is designed to achieve best results for low power and small area.
- The third library is a low power library which uses separate bulk contact to reduce the influence of supply switching noise to substrate.

Name	Category	Density ¹⁾	@ r_factor ²⁾	Main features
D_CELLS	standard	ML2: 1.3 ML3: 2.3	ML2: 2.86 ML3: 1.67	high speed
D_CELLSL	low power	ML2: 2.5 ML3: 4.6	ML2: 2.86 ML3: 1.67	min area, min power consumption
D_CELLSL_B	low power / low noise	ML2: 2.1 ML3: 3.6	ML2: 2.86 ML3: 1.67	min noise, min power consumption

- 1) averaged value: kGE/mm2 (GE = NAND2 Gate Equivalent)
ML2: 2 metal layer routing
ML3: 3 metal layer routing
- 2) average value: r_factor = Routing_factor
Place&Route_area = Cell_area * Routing_factor

> Digital I/O Cells

I/O cells are available for 5 V and 3.3 V operation voltage. Two I/O ring systems are available for pad-limited and core limited designs.

Name	Height	Pad pitch	Main features
IO_CELLS	494.9 µm	110 µm	pad limited
IO_CELLS_F	231.3 µm	variable	core limited

Input	CMOS	TTL	Pull-up	Pull-down	Output
Standard Input	■	■	■	■	
Schmitt-Trigger	■	■	■	■	
Bi-directional	■	■	■	■	1 - 8 mA (24 mA)
Slew-Rate Control Option	■	■	■	■	4 - 8 mA (24 mA)

Output	1 mA	2 mA	4 mA	8 mA	16 mA	24 mA
Standard	■	■	■	■	■	■
Slew-Rate Control Option			■	■	■	■
3-State	■	■	■	■	■	■
Open Drain	■	■	■	■	■	■

Note: Not all combinations of inputs and outputs are available as bidirectional cell. The core limited I/O library doesn't support the Slew-Rate Control Option.

> Analog Primitive Devices and Models

A very wide range of different analog primitives enable analog designers to develop sophisticated, high precision and reliable analog circuits.

High performance process modules, well defined primitives devices and accurate device models are key success factors for analog and mixed-signal design. Combined with X-FAB's CAE support kit "TheKit" and state of the art design methodologies first right mixed-signal designs are reality.

X-FAB supports BSIM3 models as the present SPICE model standard for MOS transistors. Bipolar transistors are modeled using the Gummel-Poon model. Well resistors have a non-linear terminal-voltage and bulk-voltage dependence. These resistances have to be simulated with the 3-terminal SPICE JFET model.

Model sets for most popular analog simulators, e.g. Spectre, HSPICE, ELDO and PSPICE are provided.

The same characterization and modeling effort is spent for parasitic devices and 3rd order parameters which are usually very important for analog design.

The matching behavior of MOS transistors, bipolar transistors, resistors and capacitors is very intensively investigated and characterized. Final matching parameters are extracted for all active and most of passive elements. These parameters are used at simulator model implementation for Monte Carlo simulation.

> Examples for measured and modeled parameter characteristics

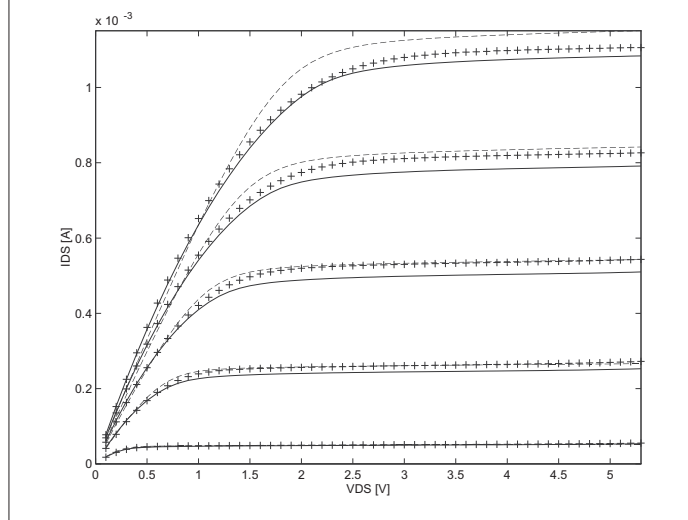


Figure 2: NMOS output characteristic of a typical wafer.
 W/L = 3/1, VGS = 1.4, 2.3, 3.2, 4.1, 5 V
 VSB = 0 V, += measured, solid line = BSIM3v3 model,
 dashed line = MOS15 model

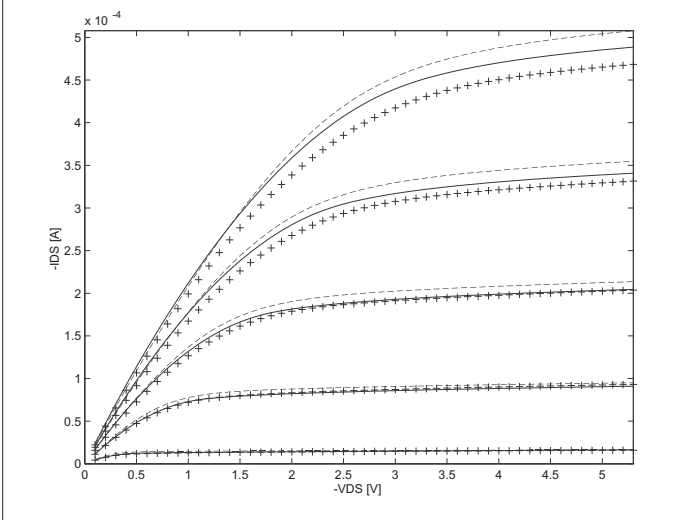


Figure 3: PMOS output characteristic of a typical wafer.
 W/L = 3/1, -VGS = 1.4, 2.3, 3.2, 4.1, 5 V
 VSB = 0 V, += measured, solid line = BSIM3v3 model,
 dashed line = MOS15 model

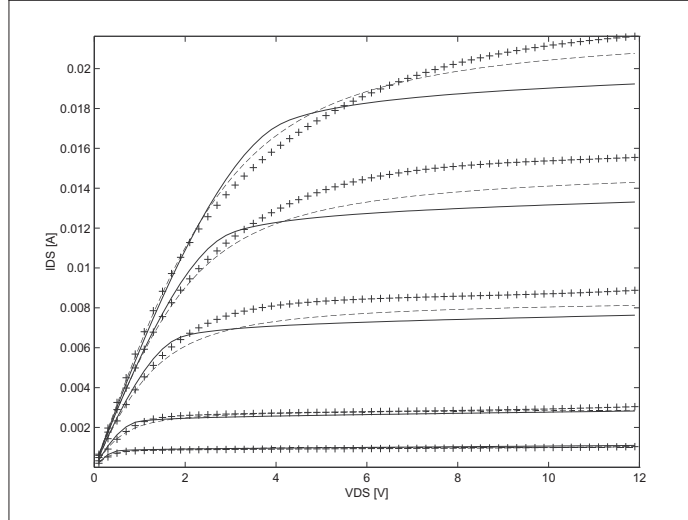


Figure 4: NMOSH output characteristic of a typical wafer.
 W/L = 125/3, VGS = 1.5, 2, 3, 4, 5 V
 VSB = 0 V, += measured, solid line = BSIM3v3 model,
 dashed line = MOS15 model

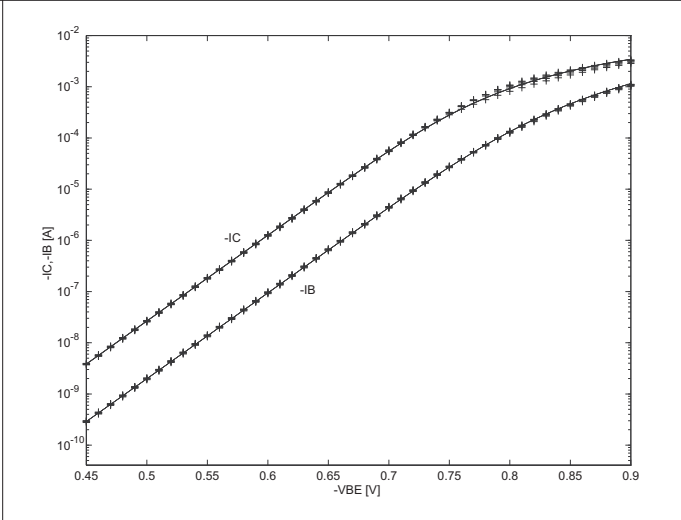


Figure 5: Gummel plot of a vertical PNP bipolar transistor (VERT15) for a typical wafer.
 VBC = 0, 1, 2, 3, 4 V, += measured,
 solid line = SPICE model

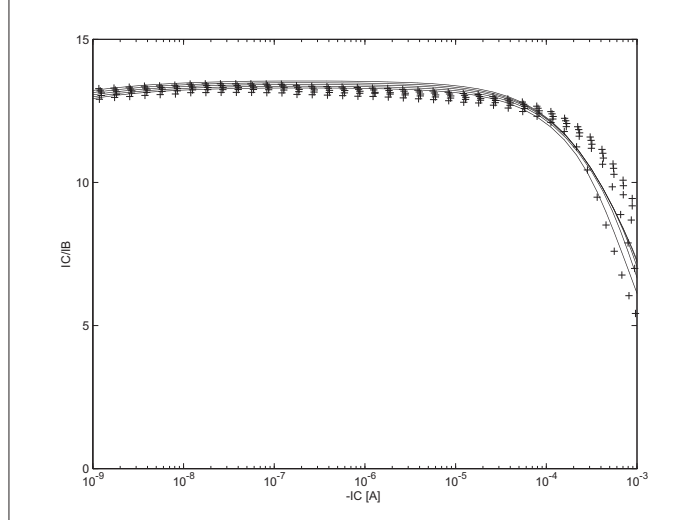


Figure 6: Current gain of vertical PNP bipolar transistor (VERT15).
 VBC = 0, 1, 2, 3, 4V, += measured,
 solid line = SPICE model

> Examples for measured and modeled parameter characteristics (continued)

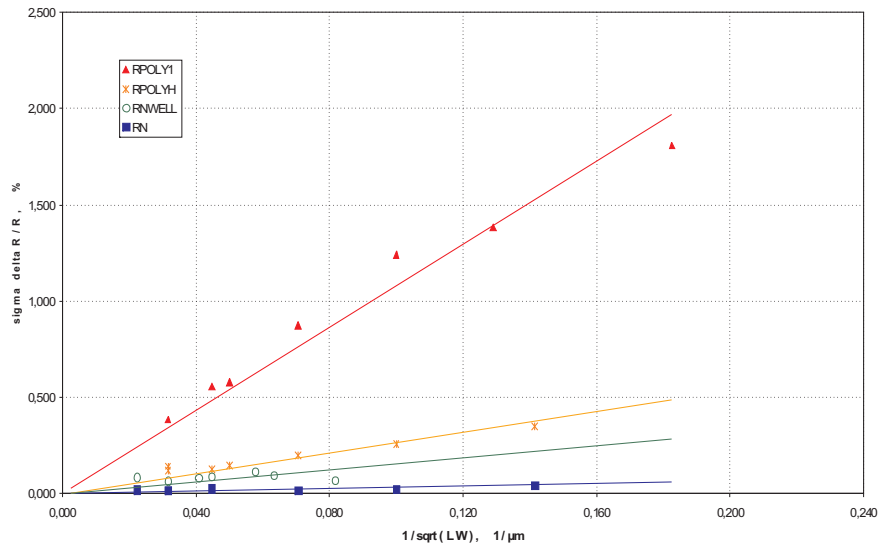


Figure 7: resistor matching

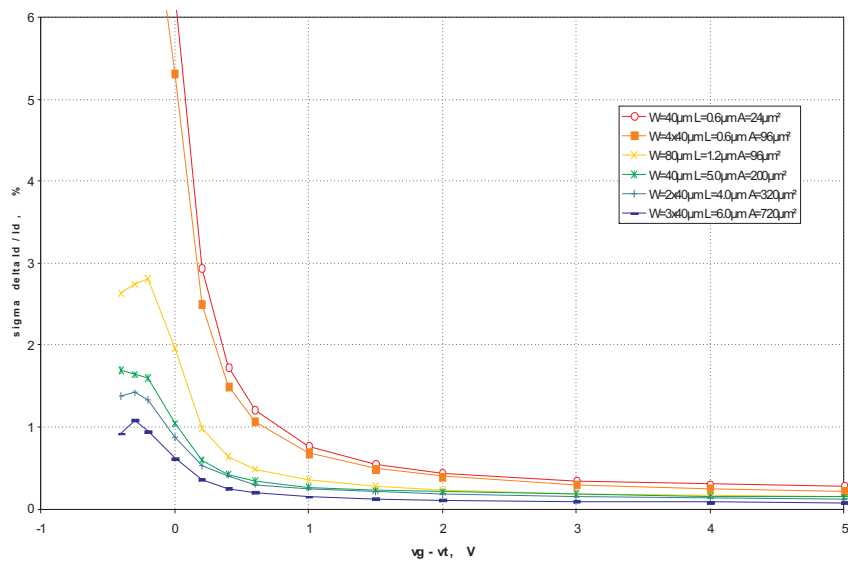


Figure 8: drain current matching CMOS

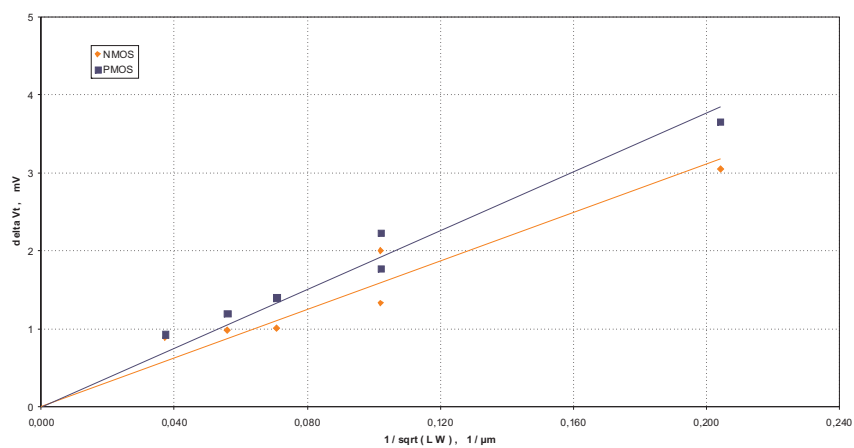


Figure 9: threshold voltage matching

> Analog Library Cells

Many analog and mixed-signal design projects are started in old technologies because designers want to re-use existing analog cells.

For easy migration to X-FAB's high performance CX06 process an increasing number of general purpose analog cells are provided.

Operational Amplifiers											
Name	V _{OL} [V]	V _{OH} [V]	V _{ICR} [V]	V _{IO} [mV]	A _{VD} [dB]	B ₁ [kHz]	SR [V/μs]	PHM [°]	I _{DD} [μA]	max. Load	Required Module
aopac01	0.1	V _{DD} -1.6	0...V _{DD} -1.5	<10	90	80	0.06/0.06	60	8	100pF/1000kΩ	CORE
aopac02	0.1	V _{DD} -1.6	0...V _{DD} -1.5	<10	90	1100	0.9/0.9	70	120	100pF/100kΩ	CORE
aopac03	0.2	V _{DD} -1.6	0...V _{DD} -1.5	<10	80	6000	8.0/7.5	60	600	10pF/10kΩ	CORE
aopac05	1.1	V _{DD} -0.1	1.5...V _{DD}	<10	90	130	0.05/0.07	70	10	100pF/1000kΩ	CORE
aopac06	1.1	V _{DD} -0.1	1.5...V _{DD}	<10	90	1200	0.8/0.9	65	110	100pF/100kΩ	CORE
aopac07	1.2	V _{DD} -0.1	1.5...V _{DD}	<10	80	7000	5.5/5.5	60	620	100pF/10kΩ	CORE
aopac09	0.05	V _{DD} -0.05	0...V _{DD} -1.5	<10	100	1400	0.7/1.0	100	250	100pF/10kΩ	CORE
aopac10	0.05	V _{DD} -0.05	0...V _{DD}	<10	100	1500	0.9/0.9	100	330	100pF/1000kΩ	CORE
aopac11	0.07	V _{DD} -0.07	1.3...V _{DD}	<10	96	4200	4.1/4.0	67	475	50pF/50kΩ	POLY2CAP
aopac12	0.05	V _{DD} -0.06	0...V _{DD} -1.7	<10	100	4000	5.0/5.4	70	490	50pF/50kΩ	POLY2CAP

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Opamps feature a standby mode.

Comparators							
Name	V _{ICR} [V]	T _{PD} for 50mV Overdrive [ns] L->H / H->L	T _{PD} for 500mV Overdrive [ns] L->H / H->L	Conditions C _L [pF]; R _L [kΩ]	Input Offset Voltage [mV]	Supply Current [μA]	Required Process Module
acmpc01	1.5 ... V _{DD}	490 / 140	260 / 160	1; 100	< 10	5	CORE
acmpc03	1.5 ... V _{DD}	140 / 20	60 / 20	1; 100	< 10	80	CORE
acmpc04	0 ... V _{DD} - 1.5	260 / 450	160 / 450	1; 100	< 10	5	CORE
acmpc06	0 ... V _{DD} - 1.5	60 / 80	20 / 80	1; 100	< 10	80	CORE
acmpc10	0 ... V _{DD}	230 / 60	150 / 75	1; 100	< 10	120	CORE
acmpc11	0 ... V _{DD}	520 / 110	320 / 130	1; 100	< 5	120	CORE

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Comparators feature a standby mode.

Bandgaps				
Name	Bandgap Voltage (unloaded) [V]; T = 30°C min / typ / max	Temperature Coefficient [ppm/°C]	Supply Current [μA]	Required Process Module
abgpc01	- / 1.275 / -	+110 ; T= -40 °C to T= 30°C +60; T= 30°C to T= 90°C	30	CORE
abgpc03	- / 1.22 / -	+50 ; T= -40 °C to T= 30°C +35; T= 30°C to T= 90°C	35	HIRES
abgpc04	- / 1.228 / -	+350; T= 25°C to T= 85°C	2	POLYCAP, HIRES

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Bandgaps feature a standby mode.

Bias Cells						
Name	Bias Voltage V _{BP} for PMOS [V]; @V _{DD} =5V, T=30°C	Temperature Coefficient IVBP [ppm / °C]	Bias Voltage V _{BN} for NMOS [V]; @V _{DD} =5V, T=30°C	Temperature Coefficient IVBN [ppm / °C]	Supply Current [μA]	Required Process Module
abiac01	V _{DD} -1.088	-500	1.28	-500	18.5	CORE
abiac02	V _{DD} -1.21	-560	1.46	-560	36	CORE
abiac03	V _{DD} -0.99	-450	1.16	-450	9.5	CORE
abiac05	-	+350	-	+450	12	POLYCAP, HIRES
abiac06	-	+4000	-	+4500	0.750	POLYCAP, HIRES

Note: All Parameters are typical, V_{DD}: 4.5 V to 5.5V, T: -40 ... 85 °C, all Bias Cells feature a standby mode.

> Analog Library Cells (continued)

Analog Switches			
Name	"ON - Resistance" typical / maximum [Ohm]	A-to-Z Propagation Delay Time [ns], @Cl= 10pF	Required Process Module
aswic01 (on chip analog signals)	100 / 500	< 10	CORE
aswic04 (external analog signals)	100 / 500	< 10	CORE
Note: All Parameters are valid for V _{DD} : 4.5 V to 5.5V, T: -4085 °C			

RC Oscillators				
Name	Frequency [kHz]	Conditions	Supply Current (specified @ V _{DD} =5V, T=25°C) [µA]	Required Process Module
arcoc01	92.0	@V _{DD} =5V; T=25°C	130	CORE
arcoc02	120 / 185 / 430	@V _{DD} =5V; T=25°C dig. code = 0000 / 1000 / 11111	38 dig. code = 1000	CORE
arcoc02f	110 / 175 / 420	@V _{DD} =5V; T=25°C dig. code = 0000 / 1000 / 11111	38 dig. code = 1000	CORE
arcoc03	10.0	@V _{DD} =5V; T=25°C	5	CORE
arcoc03f	10.0	@V _{DD} =5V; T=25°C	5	CORE
arcoc04	1000	@V _{DD} =5V; T=25°C	105	POLYCAP, HIRES
Note: All Parameters are valid for V _{DD} : 4.5 V to 5.5V, T: -4085 °C				

Crystal Oscillators				
Name	Frequency [kHz]	Supply Voltage Range V _{DD} [V]	Supply Current (specified @ V _{DD} =5V, T=25°C) [µA]	Required Process Module
axtoc10g	32	2.5 ... 3.6	0.006; @ V _{DD} =3.6V	CORE
axtoc2g	10000	4.5 ... 5.5	2.8; @ V _{DD} =5V	CORE
Note: All Parameters are valid for V _{DD} : 4.5 V to 5.5V, T: -4085 °C				

Power-On-Reset				
Name	V _{RESET_OFF} [V] (H->L Transition Voltage, Slow Voltage Rise, @5Vms) min / typ / max	T _{DEL} [µs] Delay V _{DD} -> H to POR -> L (Voltage Rise Faster than 1V/µs) typical	I _{DDL} [µA] DC-Current POR	Required Process Module
aporc01	- / 2.35 / -	6	<0.05	CORE
aporc02	- / 1.885 / -	6.5	1.7	CORE
aporc03	- / 1.6 / -	6.0 ; V _{DD} rises @>10V/µs	1.7	CORE
aporc03f	- / 1.8 / -	6.0 ; V _{DD} rises @>10V/µs	1.7	CORE
Note: All Parameters are valid for V _{DD} : 4.5 V to 5.5V, T: -4085 °C				

Analog To Digital Converter							
Name	Principle	Resolution [Bits]	Accuracy [LSB] INL / DNL	Conversion Time [Clock Cycles]	Conversion Rate [kS/s]	Input Voltage Range [V] min / max	Required Process Module
adc8	successive approximation	8	± 0.4 / ± 0.2	9	110	V _{SSA} / V _{DDA}	POLY2CAP
adc10	successive approximation	10	± 1.0 / ± 0.7	11	90	V _{SSA} / V _{DDA}	POLY2CAP
Note: All Parameters are typical, V _{DD} : 4.5 V to 5.5V, T: -4085 °C							

> Analog Library Cells (continued)

Digital To Analog Converter							
Name	Principle	Resolution [Bits]	Accuracy [LSB] INL / DNL	Output Setting Time [ns] Full Scale	Output Setting Time [ns] Code to Code	Input Voltage Range [V] min / max	Required Process Module
dac10	resistor divider	10	± 1.0 / ± 0.5	1000	230	V_{SSA} / V_{DDA}	CORE
dac8	resistor divider	8	± 0.5 / ± 0.2	800	100	V_{SSA} / V_{DDA}	CORE
dac8rs	resistor divider	8	± 0.3 / ± 0.1	150	80	V_{SSA} / V_{DDA}	CORE
dac6rs	resistor divider	6	± 0.1 / ± 0.05	60	20	V_{SSA} / V_{DDA}	CORE
adacc01	voltage scaling	10	± 1.0 / ± 0.5	300	135	V_{SSA} / V_{DDA}	CORE

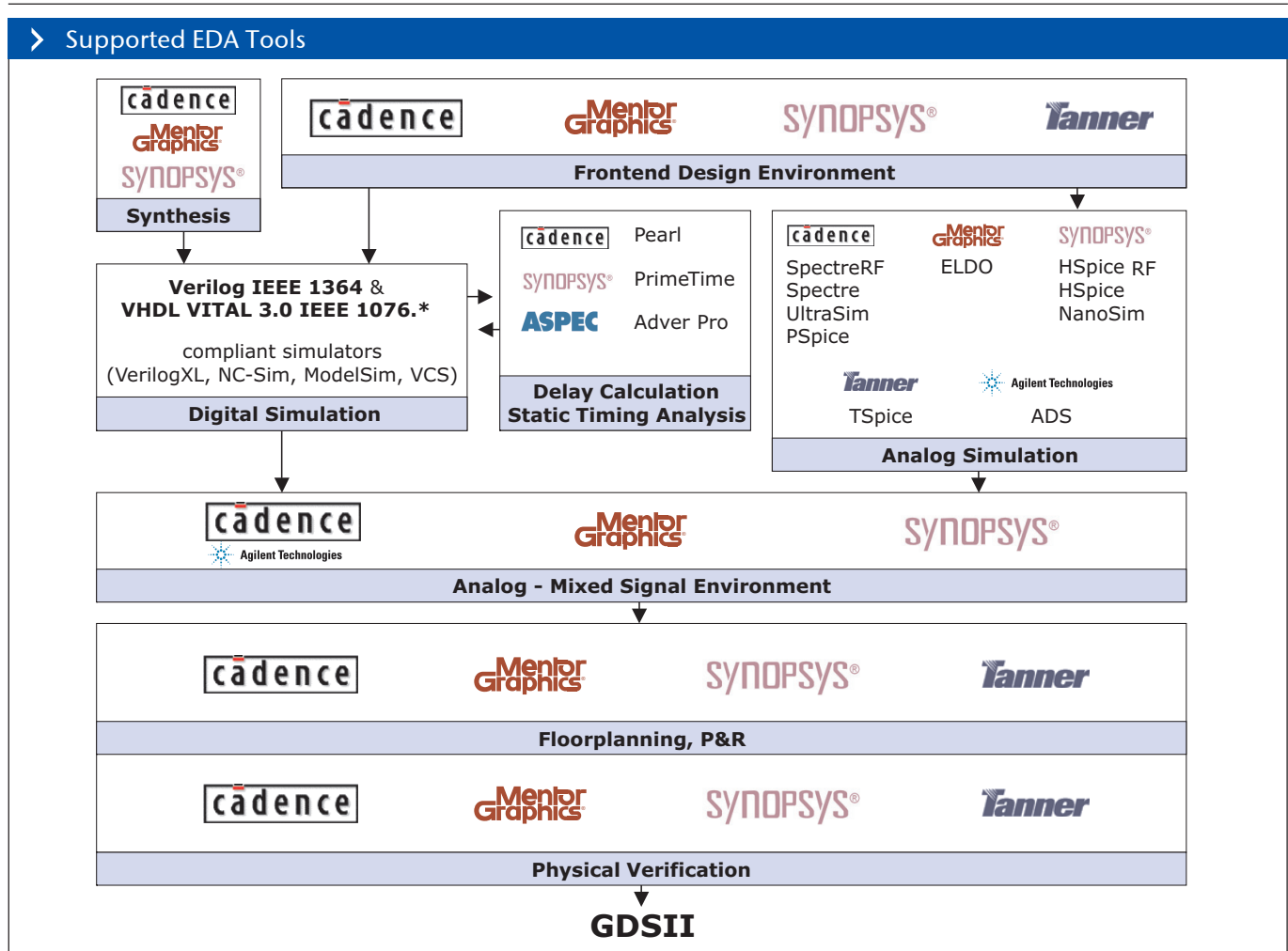
Note: All Parameters are typical, V_{DD} : 4.5 V to 5.5V, T: -40 ... 85 °C

DC-DC Converter					
Name	Input Voltage (Supply) [V] min / typ / max	Output Voltage [V] min / typ / max	Output Impedance [Ohm]	Permanent Output Current [mA] min / max	Required Process Module
adblc01g	3.0 / 3.3 / 3.6	5.5 / 5.87 / 6.0	100	0 / 6	CORE

Note: All Parameters are typical, V_{DD} : 4.5 V to 5.5V, T: -40 ... 85 °C

Schmitt-Trigger						
Name	High Threshold Voltage [V]	Low Threshold Voltage [V]	Input Frequency [kHz] max, rectangle	Supply Voltage Range [V]	Supply Current [μ A]	Required Process Module
aistc01g	$0.7 \cdot V_{DD}$	$0.3 \cdot V_{DD}$	500	2.5 ... 3.6	0.6	CORE

Note: All Parameters are typical, V_{DD} : 4.5 V to 5.5V, T: -40 ... 85 °C



> X-FAB's IC Development Kit "TheKit"

The X-FAB IC Development **Kit** is a complete solution for easy access to X-FAB technologies. TheKit is the best interface between standard CAE tools and X-FAB's processes and libraries. TheKit is available in two versions, the Master Kit and the Master Kit Plus. Both versions contain documentation, a set of software programs and utilities, digital and I/O libraries which contain full front-

end and back-end information for the development of digital, analog and mixed signal circuits. Tutorials and application notes are included as well. The Master Kit Plus additionally provides a set of general purpose analog functions mentioned in section "Analog Library Cells" and is subject to a particular license.

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